

LOW POWER DC-DC CONVERTERS AND A LOW QUIESCENT POWER
HIGH PSRR CLASS-D AUDIO AMPLIFIER

A Dissertation

by

JOSELYN TORRES

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	José Silva-Martínez
	Prasad Enjeti
	César Malavé
Head of Department,	Chanan Singh

December 2013

Major Subject: Electrical Engineering

Copyright 2013 Joselyn Torres

ABSTRACT

High-performance DC-DC voltage converters and high-efficient class-D audio amplifiers are required to extend battery life and reduce cost in portable electronics. This dissertation focuses on new system architectures and design techniques to reduce area and minimize quiescent power while achieving high performance. Experimental results from prototype circuits to verify theory are shown.

Firstly, basics on low drop-out (LDO) voltage regulators are provided. Demand for system-on-chip solutions has increased the interest in LDO voltage regulators that do not require a bulky off-chip capacitor to achieve stability, also called capacitor-less LDO (CL-LDO) regulators. Several architectures have been proposed; however, comparing these reported architectures proves difficult, as each has a distinct process technology and specifications. This dissertation compares CL-LDOs in a unified manner. Five CL-LDO regulator topologies were designed, fabricated, and tested under common design conditions.

Secondly, fundamentals on DC-DC buck converters are presented and area reduction techniques for the external output filter, power stage, and compensator are proposed. A fully integrated buck converter using standard CMOS technology is presented. The external output filter has been fully-integrated by increasing the switching frequency up to 45 MHz. Moreover, a monolithic single-input dual-output buck converter is proposed. This architecture implements only three switches instead of the four switches used in conventional solutions, thus potentially reducing area in the power stage through proper design of the power switches. Lastly, a monolithic PWM voltage mode buck converter with compact Type-III compensation is proposed. This compensation scheme employs a combination of Gm-RC and Active-RC

techniques to reduce the area of the compensator, while maintaining low quiescent power consumption and fast transient response. The proposed compensator reduces area by more than 45% when compared to an equivalent conventional Type-III compensator.

Finally, basics on class-D audio amplifiers are presented and a clock-free current-controlled class-D audio amplifier using integral sliding mode control is proposed. The proposed amplifier achieves up to 82 dB of power supply rejection ratio and a total harmonic distortion plus noise as low as 0.02%. The IC prototype's controller consumes 30% less power than those featured in recently published works.

DEDICATION

To my parents Aida and Miguel,
my aunt Irma, and my grandmother Maya

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor, Dr. Edgar Sánchez-Sinencio for his guidance, patience, and encouragement throughout the course of my research. I would also like to thank Dr. José Silva-Martínez, Dr. Prasad Enjeti, and Dr. César Malavé for serving on my committee.

I have had the pleasure of collaborating in research projects with: Miguel Rojas-González, Adrian Colli-Menchi, Mohamed El-Nozahi, Ahmed Amer, Seenu Gopalraju, Reza Abdullah, Xiaosen Liu, Chao Zhang, Jun Yan, and Hui Chen. Many thanks to all of you. I also want to thank Ella Gallagher and Tammy Carda for their invaluable assistance.

I would like to thank all my colleagues in the AMSC group; especially Salvador Carreon, Fernando Lavallo, Jorge Zarate, Félix Fernández, Raghavendra Kulkarni, and Erik Pankratz for their friendship and valuable research discussions.

I am grateful to my best friend Luz for her comprehension and constant support during these years. Finally, I want to express my deepest gratitude to my parents Aida and Miguel, and my sisters Zobeida and Mirayda, for their unconditional love and support throughout my entire life.

TABLE OF CONTENTS

	Page
ABSTRACT	ii
DEDICATION	iv
ACKNOWLEDGEMENTS	v
TABLE OF CONTENTS	vi
LIST OF FIGURES	xi
LIST OF TABLES	xix
1. INTRODUCTION	1
1.1 Motivation and Goals	1
1.2 Organization	1
1.2.1 DC-DC Converters	1
1.2.2 Class-D Audio Amplifiers	3
2. INTRODUCTION TO DC-DC CONVERTERS	4
2.1 Introduction	4
2.2 Low-Power DC-DC Converters	5
2.3 Types of DC-DC Voltage Converters	6
2.3.1 Linear Voltage Regulator	6
2.3.2 Switching-Inductor Converters	7
2.3.3 Switching Capacitor Converters	8
2.3.4 DC-DC Converters Comparison	10
3. LOW DROP-OUT VOLTAGE REGULATORS	12
3.1 Introduction	12
3.2 Basic Analysis	12
3.3 Design Specifications	13
3.3.1 Stability	14
3.3.2 Load Transient	15
3.3.3 Load Regulation	15
3.3.4 Power Supply Rejection (PSR)	16
3.3.5 Line Transient and Regulation	20
3.3.6 Noise	22
3.3.7 Quiescent Current	24

3.3.8	Drop-Out Voltage	24
3.3.9	Efficiency	24
3.4	Externally Compensated LDO Voltage Regulators	25
3.4.1	Stability	26
3.4.2	Load Transient	27
3.4.3	Power Supply Rejection	29
3.5	Internally Compensated LDO Voltage Regulators	31
3.5.1	Stability	32
3.5.2	Load Transient	36
3.5.3	Power Supply Rejection	41
3.5.4	PMOS Versus NMOS Pass Transistor	44
3.6	Externally Versus Internally Compensated LDO Voltage Regulators .	46
3.7	Guidelines for Measuring LDO Voltage Regulators	47
3.7.1	Efficiency Measurement Setup	47
3.7.2	Load Transient Measurement Setup	47
3.7.3	Line Transient Measurement Setup	48
3.7.4	PSR Measurement Setup	48
3.8	Design Strategy in LDO voltage regulators	49
3.9	Practical Design Considerations for LDO Voltage Regulators	51
3.9.1	Pass Transistor	51
3.9.2	Error Amplifier	53
3.9.3	Printed Board Circuit	55
4.	LOW DROP-OUT VOLTAGE REGULATORS: CAPACITOR-LESS ARCHITECTURE COMPARISON	57
4.1	Introduction	57
4.2	Comparison of CL-LDO Regulator Topologies	57
4.2.1	Advanced Compensation Topologies	58
4.2.2	Load Transient Topologies	59
4.2.3	PSR Topologies	62
4.3	Selected Topologies	65
4.4	Experimental Results	70
4.4.1	Quiescent Current and Stability	71
4.4.2	Load Transient/Regulation	73
4.4.3	PSR	74
4.4.4	Line Transient/Regulation	75
4.4.5	Noise	77
4.5	Conclusion	79
5.	FUNDAMENTALS OF INDUCTOR SWITCHING DC-DC CONVERTERS	81
5.1	Introduction	81
5.2	Non-Isolated versus Isolated DC-DC switching converters	81
5.3	Buck Converter Operation	82

5.4	Buck Converter Output Filter Component Selection	86
5.4.1	Output Inductor	86
5.4.2	Output Capacitor	86
5.5	Efficiency in Buck Converters	88
5.5.1	Conduction Power Losses	90
5.5.2	Dynamic Power Losses	91
5.5.3	Gate Drive Power Losses	91
5.5.4	Body Diode Power Losses	92
5.5.5	Quiescent Power Losses	92
5.5.6	Short Circuit Power Losses	93
5.6	Main Control Schemes	93
5.6.1	Voltage Mode PWM Compensation	93
5.6.2	Current Mode PWM Compensation	104
5.6.3	Hysteretic Compensation	110
5.6.4	Sliding Mode Control Compensation	112
5.6.5	Digital Control Compensation	116
5.6.6	Compensation Scheme Summary	118
5.7	Multiphase Interleaved Buck Converter	118
5.8	Practical Design Considerations for Switching Converters	121
5.8.1	Building Blocks	121
5.8.2	Printed Circuit Board	127
5.9	Measurements	128
5.9.1	Efficiency Measurement Setup	129
5.9.2	Load Transient Measurement Setup	129
5.9.3	Line Transient Measurement Setup	130
6.	AREA REDUCTION TECHNIQUES FOR BUCK CONVERTERS	132
6.1	Introduction	132
6.2	Buck Converter Output Filter Area Reduction	133
6.2.1	Multi-Phase Interleaved Buck Converter	134
6.2.2	Proposed Dual-Phase Buck Converter Architecture	135
6.2.3	Integrated Output Low-Pass Filter	136
6.2.4	Simulation Results	139
6.3	Buck Converter Power Stage Area Reduction	142
6.3.1	Multiple-Output Buck Converter	143
6.3.2	Dual-Output Operation	143
6.3.3	Multiple-Output Operation	145
6.3.4	Proposed Dual-Output Buck Converter Architecture	146
6.3.5	Digital Logic Circuit	146
6.3.6	Output Power Stage	148
6.3.7	Simulation and Experimental Results	150
6.3.8	Steady-State Operation of the System	150
6.3.9	Transient Operation of the System	154
6.4	Buck Converter Compensator Area Reduction	157

6.4.1	Proposed Compact Compensation	159
6.4.2	Building Blocks Implementation	165
6.4.3	Experimental Results	173
6.5	Conclusion	177
7.	INTRODUCTION TO CLASS-D AUDIO AMPLIFIERS	179
7.1	Introduction	179
7.2	Types of Audio Amplifiers	179
7.2.1	Class-A	179
7.2.2	Class-B	180
7.2.3	Class-AB	180
7.2.4	Class-D	180
7.2.5	Class-G	180
7.3	Class-D Audio Amplifiers	181
7.3.1	Open Loop Class-D Audio Amplifier	181
7.3.2	Closed Loop Architecture	186
7.3.3	Digital Class-D Audio Amplifiers	191
7.3.4	Filter-Less Class-D Audio Amplifiers	192
7.3.5	Performance Metrics of Class-D Audio Amplifiers	193
7.3.6	Total Harmonic Distortion	195
7.3.7	Total Harmonic Distortion Plus Noise	196
7.3.8	Signal-to-Noise Ratio	197
7.3.9	Power Supply Rejection Ratio and Power Supply Intermodulation Distortion	197
7.3.10	Practical Considerations	198
8.	A LOW QUIESCENT POWER HIGH-PSRR CLASS-D AUDIO AMPLIFIER	199
8.1	Introduction	199
8.2	Design of the Proposed Class-D Architecture	202
8.3	Building Blocks Implementation	204
8.3.1	Integral Sliding Mode Controller	204
8.3.2	Hysteretic Comparator	208
8.3.3	Output Power Stage	210
8.3.4	Output Filter	211
8.4	Experimental Results	211
8.5	Conclusion	215
9.	SUMMARY	217
	REFERENCES	218
	APPENDIX A. LDO VOLTAGE REGULATOR PERFORMANCE DEFINITIONS	238

APPENDIX B. FUNDAMENTALS OF SLIDING MODE CONTROL	240
APPENDIX C. STABILITY ANALYSIS OF THE CLASS-D AUDIO AMPLIFIER	254

LIST OF FIGURES

FIGURE		Page
2.1	DC-DC converter block diagram.	5
2.2	Linear voltage regulator block diagram (a) conceptual (b) pass element implementation.	6
2.3	Simplified buck converter implementation.	8
2.4	Simplified switched capacitor voltage regulator implementation ($V_{OUT} = 2V_{IN}$).	9
2.5	Example of a power management system for portable applications. . .	10
3.1	(a) Basic LDO voltage regulator topology (b) small signal representation.	13
3.2	LDO voltage regulator setup for stability analysis.	14
3.3	Load transient simulation setup.	15
3.4	Simplified block diagram of a LDO voltage regulators including PCB trace and bonding wire parasitics.	17
3.5	General conceptual block diagrams for (a) an amplifier (b) LDO voltage regulator.	18
3.6	Input-to-output ripple paths in LDO regulators [10].	18
3.7	(a) Small signal model for PSR of Type-A amplifiers and (b) transistor level example of Type-A amplifier [12].	19
3.8	(a) Small signal model for PSR of Type-B amplifiers and (b) an example of Type-B error amplifier [12].	20
3.9	LDO regulator's major noise contributors.	22
3.10	Externally compensated LDO voltage regulator with PMOS pass transistor.	25
3.11	Small-signal model for an externally compensated LDO voltage regulator with PMOS pass transistor.	26

3.12	Externally compensated LDO voltage regulator with PMOS pass transistor Bode plot.	28
3.13	Equivalent circuit for load transient analysis.	29
3.14	PSR small signal model for externally compensated LDO voltage regulator with PMOS pass transistor and Type-A EA.	30
3.15	PSR small signal model for externally compensated LDO voltage regulator with PMOS pass transistor and Type-B EA.	30
3.16	Internally compensated LDO voltage regulator with (a) PMOS and (b) NMOS pass transistors.	32
3.17	Small signal model for internally compensated LDO voltage regulator with PMOS pass transistor.	33
3.18	(a) Internally compensated LDO voltage regulator with PMOS pass transistor Bode plot (b) schematic utilized to obtain (a).	34
3.19	Small signal model for internally compensated LDO voltage regulator with NMOS pass transistor.	35
3.20	(a) Internally compensated LDO voltage regulator with NMOS pass transistor Bode plot and (b) schematic utilized to obtain (a).	37
3.21	Output impedance at DC versus load current.	39
3.22	M_P parasitic capacitance versus load current.	40
3.23	Reduction in output voltage undershoot amplitude versus bias current.	40
3.24	PSR small signal model for internally compensated LDO voltage regulator with PMOS pass transistor and Type-A EA.	41
3.25	PSR small signal model for internally compensated LDO voltage regulator with PMOS pass transistor and Type-B EA.	41
3.26	PSR small-signal model for externally compensated LDO voltage regulator with NMOS pass transistor and Type-A EA.	43
3.27	PSR small-signal model for internally compensated LDO voltage regulator with NMOS pass transistor and Type-B EA.	43
3.28	Internally compensated LDO voltage regulator PSR.	45
3.29	Load transient measurement setup.	48

3.30	Line transient measurement setup.	49
3.31	Low dropout voltage regulator design flow.	50
3.32	Example of an error amplifier (a) transistor level (b) layout implementation.	55
3.33	Off-chip capacitor model that includes R_{ESR} and ESL	56
4.1	CL-LDOs with improved frequency compensation techniques (a) DFC [18], (b) Q-Reduction [23].	58
4.2	CL-LDOs with multi-feedback loops (a) Differentiator [26], (b) Transimpedance [25], (c) High Slew Rate EA [29], (d) AFC&SRE [30], (e) Adaptively Biased [32], and (f) Capacitive Coupling & ATC [33]. . .	60
4.3	CL-LDOs based on FVF [35]-[39].	62
4.4	CL-LDOs for PSR enhancement (a) NMOS Cascode [40], (b) NMOS Cascode with auxiliary LDO [41, 42], (c) Voltage Subtractor [24], (d) FF with BPF [44].	63
4.5	CL-LDO regulator with damping factor technique small-signal model.	64
4.6	CL-LDO regulator with Q-reduction technique small-signal model. . .	65
4.7	CL-LDO regulator with voltage subtractor technique small-signal model.	66
4.8	CL-LDO regulator with transimpedance technique small-signal model.	66
4.9	CL-LDO regulator with differentiator technique small-signal model. .	67
4.10	Load transient experimental results.	73
4.11	PSR measurement results for $I_L=100\mu A$	75
4.12	PSR measurement results for $I_L=50mA$	76
4.13	Line transient experimental results.	77
4.14	Output noise spectral density simulation results.	78
5.1	Buck converter in (a) asynchronous (b) synchronous.	83
5.2	Buck converter operating in (a) continuous conduction mode (CCM) (b) discontinuous conduction mode (DCM).	84
5.3	Buck converter's voltage conversion ratio (V_{OUT}/V_{IN}) versus D for different K values.	85

5.4	Buck converter (a) output voltage and (b) load current waveforms during a load transient event.	87
5.5	Equivalent buck converter for load transient analysis.	88
5.6	Buck converter power losses sources.	89
5.7	Block diagram of a buck converter with voltage mode PWM control. .	94
5.8	Buck converter's output filter with parasitics.	95
5.9	Open loop Bode plot without compensation block.	96
5.10	Type-I compensator implementation.	97
5.11	Type-I compensator Bode plot.	98
5.12	Type-II compensator implementation.	99
5.13	Type-II compensator Bode plot.	100
5.14	Conventional Type-III compensation.	101
5.15	Conventional Type-III Bode plot.	102
5.16	Buck converter with peak current mode control block diagram. . . .	104
5.17	A typical compensation implementation of $H(s)$ for current mode control.	105
5.18	Series sense resistor.	107
5.19	Filter sense the inductor.	108
5.20	Sense Fet method.	109
5.21	Block diagram of a buck converter with hysteretic compensation. . .	110
5.22	Hysteretic comparator.	112
5.23	Block diagram of a buck converter implemented with sliding mode control.	113
5.24	Subintervals in a buck converter (a) subinterval I (b) subinterval II. .	114
5.25	Phase portraits of V_{OUT} (a) phase portrait of structure I and (b) phase portrait of structure II.	115
5.26	Phase portrait of the controlled system trajectories of V_{OUT} under sliding-mode operation.	116

5.27	Block diagram of a buck converter with digital control.	117
5.28	Multiphase interleaved buck converter.	119
5.29	Output current ripple versus duty cycle for different N values.	120
5.30	Transistor level of the comparator.	122
5.31	A common comparator in buck converter without hysteresis.	123
5.32	Carrier signal generator circuit.	124
5.33	Non-overlapping circuit.	125
5.34	PCB design recommendations.	128
5.35	Efficiency measurement setup for a buck converter.	129
5.36	Load transient measurement setup for a buck converter.	130
5.37	Line transient measurement setup for a buck converter.	131
6.1	Block diagram of the buck converter.	132
6.2	Proposed fully-integrated voltage regulator architecture.	135
6.3	MOSCAP implementation.	137
6.4	Extracted schematic inductor model.	138
6.5	Layout of the proposed fully-integrated buck converter.	140
6.6	Efficiency versus P_{OUT} of the proposed buck converter.	140
6.7	Efficiency versus Q_L	141
6.8	Output voltage variation for a current step from 100 mA to 200 mA and vice versa.	141
6.9	Multiple supplies on a typical system.	142
6.10	Schematic diagram of the dual-output buck voltage regulator and its operating modes (a) subinterval I (b) subinterval II and (c) subinterval III.	144
6.11	Sequence of non-overlapping operating signals applied to T_1 , T_2 , and T_3 , in the dual-output buck voltage converter.	144
6.12	Single-input multiple-output converter.	145

6.13	Block diagram of the proposed dual-output buck voltage converter.	146
6.14	(a) Simplified digital logic to generate G_1 , G_2 , and G_3 and (b) Buck converter switching signals PWM_1 and PWM_2	147
6.15	Transistor level implementation of the bootstrapping circuit.	149
6.16	Dual-output buck voltage regulator IC micrograph.	150
6.17	Measured (a) control signals G_1 , G_2 , and G_3 and (b) pulse-width modulated signals.	151
6.18	(a) Power efficiency measurements of the dual-output buck voltage versus both output currents and (b) top view of (a).	152
6.19	Load regulation when (a) 100 mA step is applied to I_{OUT1} while I_{OUT2} is fixed at 0 mA and (b) I_{OUT1} is fixed at 0 mA while 100 mA step is applied I_{OUT2}	153
6.20	Line regulation with V_{IN} (V_{DD}) step from 1.8 V to 2.5 V (refer to Figure 6.13).	155
6.21	(a) 25 mA step is applied to I_{OUT1} while I_{OUT2} is fixed at 60 mA and (b) I_{OUT1} is fixed at 60 mA while 25 mA step is applied I_{OUT2}	155
6.22	Block diagram of a voltage mode PWM buck converter.	157
6.23	(a) Block and (b) circuit diagrams of the proposed compensator.	159
6.24	Proposed compensator Bode plot.	161
6.25	Buck converter open loop frequency response with the proposed compensator (a) gain (b) phase.	162
6.26	Loop phase margin with proposed compensator versus process corners.	163
6.27	Area distribution of a buck converter implemented with: (a) conventional Type-III compensator and (b) proposed compensator.	164
6.28	Gm-RC section transistor level implementation.	165
6.29	Comparator transistor level implementation.	168
6.30	Carrier signal generator implementation.	169
6.31	Carrier signal waveform.	170
6.32	Power stage block diagram.	172

6.33	Buck converter die micrograph, I compensator (0.0985mm^2), II comparator and carrier signal generator (0.0073mm^2), and III power stage (0.0267mm^2).	174
6.34	Efficiency versus output power.	174
6.35	Measurement setup for (a) load transient and (b) line transient. . . .	175
6.36	Load transient response (x-axis = $20\mu\text{s}/\text{div}$, V_{OUT} y-axis = $50\text{mV}/\text{div}$, and I_L y-axis = $200\text{mV}/\text{div}$).	176
6.37	Line transient response (x-axis = $50\mu\text{s}/\text{div}$, V_{OUT} y-axis = $20\text{mV}/\text{div}$, and V_{IN} y-axis = $1\text{V}/\text{div}$).	177
7.1	Single-ended open loop class-D audio amplifier architecture.	182
7.2	System block diagram for the synchronous buck converter or class-D audio amplifier in closed loop.	184
7.3	Differential open loop class-D audio amplifier architecture.	185
7.4	(a) Two-level (b) three-level modulation signals.	186
7.5	Single-ended PWM closed loop class-D audio amplifier architecture. .	187
7.6	Single-ended closed loop $\Delta\Sigma$ class-D audio amplifier architecture. . .	188
7.7	Single-ended closed loop hysteretic class-D audio amplifier architecture.	189
7.8	Class-D audio amplifier based on sliding mode control block diagram.	191
7.9	Audio system with (a) analog and (b) digital input class-D audio amplifier.	192
7.10	Filter-less class-D audio amplifier with BD-modulation.	193
7.11	Simplified loudspeaker model.	193
7.12	Testbench setup for efficiency measurements.	194
7.13	Testbench setup for THD, THD+N, and SNR measurements.	195
7.14	Testbench for PSRR and PS-IMD measurements.	197
8.1	Conventional PWM class-D audio amplifier.	200
8.2	Single-bit $\Delta\Sigma$ class-D audio amplifier architecture.	200

8.3	Self-oscillating class-D audio amplifier architecture.	201
8.4	Sliding mode control class-D audio amplifier architecture.	201
8.5	Block diagram of the proposed class-D amplifier.	202
8.6	Proposed class-D audio amplifier implementation, I ISMC, II comparator, III output power stage, IV LPF.	204
8.7	Efficiency versus R_s for $V_{in} = 2 V_{pp}$	206
8.8	THD versus GBW of the current sensing amplifier (A_2).	207
8.9	Fully differential two-stage amplifier implementation.	208
8.10	Hysteretic comparator implementation.	209
8.11	Average switching frequency versus normalized input amplitude ($\frac{V_{in,peak}}{V_{FS}}$, where $V_{FS} = 2.7$ V).	210
8.12	Class-D amplifier die micrograph, I controller (0.430mm^2), II com- parator (0.033mm^2), and III output stage (1.190mm^2).	211
8.13	(a) Power and (b) area distribution of the proposed audio amplifier. .	212
8.14	Class-D audio amplifier output FFT when $V_{in} = 2.82 V_{pp}$ at 1 kHz. .	213
8.15	Class-D audio amplifier a) THD+N and b) efficiency versus output power.	213
8.16	Class-D audio amplifier PSRR and SNR versus frequency.	214
8.17	Power supply induced intermodulation distortion measurement. . . .	215
B.1	Model of a simple variable structure system.	241
B.2	Phase portraits of the second-order system in equation (B.1) for (a) Re- gion I when $s(x_1, x_2, t) < 0$ and (b) Region II when $s(x_1, x_2, t) > 0$. .	243
B.3	Phase portrait of the second-order system in equation (B.1) with slid- ing mode.	244
C.1	Class-D amplifier output filter.	255

LIST OF TABLES

TABLE		Page
2.1	DC-DC converters comparison	10
3.1	Type-A and Type-B single stage amplifier characteristics	21
3.2	Analytical expressions for PSR of an externally compensated LDO voltage regulator	31
3.3	Externally versus internally compensated LDO voltage regulators output impedance comparison	38
3.4	Analytical expressions for PSR of an internally compensated LDO voltage regulator with PMOS Pass Transistor	42
3.5	Analytical expressions for PSR of an internally compensated LDO voltage regulator with NMOS Pass Transistor	44
3.6	PMOS versus NMOS pass transistor comparison	45
3.7	Externally versus internally compensated LDO voltage regulators comparison	46
4.1	CL-LDO regulator loop small signal parameters ($A_{EA,o}$, ω_{p1} , ω_o) . . .	68
4.2	CL-LDO regulator loop small signal parameters (Q , ω_{z1} , ω_{p4})	68
4.3	CL-LDO regulators PSR analytical expressions	69
4.4	Targeted design specifications for the CL-LDO regulators	71
4.5	Measurement performance summary of the designs in $0.5\mu\text{m}$ CMOS technology	72
4.6	Differential pair area (W·L) for each selected topology	79
4.7	CL-LDO qualitative features	79
5.1	CCM versus DCM	85
5.2	Summary of advantages and disadvantages of the different compensation schemes	118

6.1	Component values of the schematic inductor model	139
6.2	Comparison of dual-output buck voltage regulators	156
6.3	Component's value of compensation implementations	163
6.4	Buck converter performance summary	175
8.1	Performance summary	216

1. INTRODUCTION

1.1 Motivation and Goals

There is an imperative demand for high performance electronic circuits with high efficiency and low quiescent power consumption to extend battery life and reduce cost in portable devices. In addition, miniaturization of electronic circuits is also a critical aspect due to the limited space in portable applications. In this work, we focus on DC-DC converters and audio amplifiers since they are fundamental building blocks in almost every portable device. The main goal of this dissertation is to reduce area and quiescent power consumption while maintaining low cost and high performance.

1.2 Organization

This dissertation is divided as follows: the first part discusses the fundamentals, design, implementation, and testing methods of DC-DC converters. The second part of this dissertation presents the principles of class-D audio amplifiers, as well as the design, implementation, and testing of a class-D audio amplifier.

1.2.1 DC-DC Converters

An introduction to DC-DC converters and the different types of low-power DC-DC converter topologies is presented in Section 2. Section 3 describes low drop-out (LDO) voltage regulators implemented in CMOS processes. In addition, design specifications, guidelines for measuring, and practical design considerations for LDO voltage regulators are discussed.

A comparative study of LDO voltage regulators that do not require a bulky off-chip capacitor to achieve stability, also called capacitor-less LDO (CL-LDO) regulators, is presented in Section 4. A number of architectures have been proposed;

however, comparing these architectures proves difficult, as each has a distinct process technology and specifications. This section compares CL-LDO regulators in a unified manner. We designed, fabricated, and tested five illustrative CL-LDO regulator topologies under common design conditions in $0.5\ \mu\text{m}$ CMOS technology. We compared the architectures in terms of (1) line/load regulation, (2) power supply rejection, (3) line/load transient, (4) total on-chip compensation capacitance, (5) noise, and (6) quiescent power consumption. Insights on what optimal topology to choose to meet particular LDO specifications are provided.

Fundamentals of buck converters are introduced in Section 5. Moreover, the main topologies and control schemes for buck converters are described. Practical design considerations for buck converters are also included.

In Section 6, area reduction techniques for the output filter, output power stage, and compensator of the buck converter are presented. The design and simulation results of a fully-integrated buck converter using $0.18\ \mu\text{m}$ CMOS technology are shown. The proposed converter is a monolithic solution, based on standard CMOS technology, for integration of passive components on-chip without the need of expensive and complicated post-fabrication processes. Practical design limitations have been found and possible solutions to overcome these challenges are provided. The design, implementation, and testing of an integrated, single-input, dual-output buck converter is presented. This topology implements only three switches instead of four switches in conventional solutions, and can reduce area in the power stage with proper design of the power switches. The integrated circuit prototype was fabricated in standard $0.5\ \mu\text{m}$ CMOS technology ($V_{\text{THN}} \approx 0.78\ \text{V}$, $V_{\text{THP}} \approx -0.93\ \text{V}$) and experimental results are also shown. Finally, a PWM voltage mode buck converter with compact Type-III compensation is proposed. This compensation scheme employs a combination of Gm-RC and Active-RC techniques to emulate the conventional Type-III compensa-

tion. The introduced compensator occupies less area than an equivalent conventional Type-III topology and as a result, the total active area of the buck converter is reduced. The prototype was fabricated in $0.18\ \mu\text{m}$ CMOS standard technology and measurement results show fast settling time and high efficiency performance.

1.2.2 *Class-D Audio Amplifiers*

Section 7 covers the basics on class-D audio amplifiers and principles of operation. Furthermore, the similarities between the synchronous buck converter and class-D audio amplifier will be demonstrated. In addition, the main class-D topologies and performance metrics are presented. Practical design considerations at the integrated and printed circuit level are also provided.

A low power, high PSRR, clock-free, current-controlled class-D audio power amplifier is proposed in Section 8. The proposed audio amplifier utilizes integral sliding mode control (ISMC) to ensure robust operation. This architecture has two feedback loops: 1) an outer voltage loop that minimizes the voltage error between the input and output audio signals, and 2) an inner current loop that measures the inductor current to track the input signal accurately. The IC prototype's controller consumes less power than those featured in recently published works. Experimental results of the prototype are shown.

Finally, Section 9 summarizes the contributions of this dissertation and discusses future work.

2. INTRODUCTION TO DC-DC CONVERTERS

2.1 Introduction

The power management integrated circuit (IC) market is expected to grow from \$32.2 billion in 2013 and to \$38.7 billion in 2016 [1]. This demand is driven partially by portable devices such as smart phones and media tablets. Power management circuits include voltage regulators (DC-DC converters), voltage references, and power transistors among others. The voltage regulator market is expected to grow at 5.2% annually from \$9.5 billion in 2012 to \$12.3 billion in 2017.

DC-DC converters convert a DC input voltage to a secondary DC output voltage level. These converters are essential building blocks in electronic circuits since almost every system requires a regulated voltage supply. Furthermore, multiple DC-DC converters are often required in modern electronics systems because their subsystems may demand different voltage and current specifications [2]. A DC-DC converter must mainly provide high efficiency, fast transient response, and good voltage regulation.

The required power delivered by DC-DC converters depends on the application. For instance, the power delivered to the load in portable applications is typically in the range of few watts, whereas DC-DC converters for computers may provide an output power in the order of hundreds of watts. Moreover, in a variable speed motor driver application, the power delivered to the load can be as high as megawatts [2].

This chapter is organized as follows: Section 2.1 describes the basic operation principles of low-power DC-DC converters. Section 2.2 presents different types of low-power DC-DC converters and their main characteristics.

2.2 Low-Power DC-DC Converters

DC-DC converters typically operate in a closed loop fashion to minimize the effect of load perturbations and/or input voltage variations which could affect the output voltage [3]. A conceptual DC-DC converter block diagram is shown in Figure 2.1.

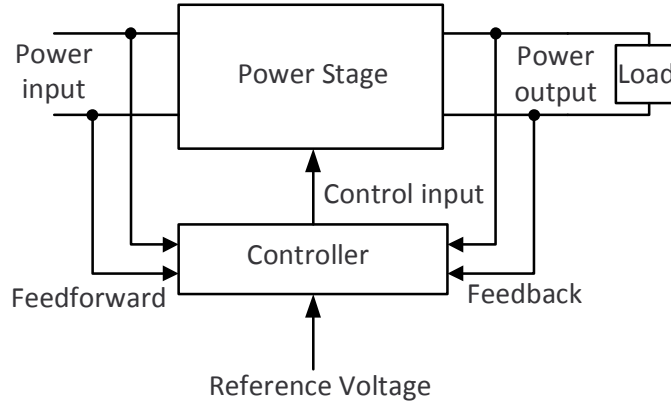


Figure 2.1: DC-DC converter block diagram.

It consists of a power stage, a controller which uses the feedforward/feedback paths information to control the power stage, and a reference voltage. Voltage regulation is achieved by sensing the output/input variations of the DC-DC converter and feeding them back/forward to the controller block. The controller circuit generates a control signal to minimize the error between the reference and output voltages. Low power DC-DC converters can be classified in: linear voltage regulators, switching-inductor converters, and switching-capacitor converters. In linear voltage regulators, the power stage operates as an amplifier; while in switching-inductor and switching-capacitor converters, the pass element operates as an electronic switch that is either on or off.

2.3 Types of DC-DC Voltage Converters

2.3.1 Linear Voltage Regulator

Linear voltage regulators (LVRs) are popular due to their simpler implementation and smaller area when compared with other types of DC-DC converters. In addition, they are preferred to power noise sensitive circuits since they can provide a low noise output voltage. LVRs can generate an output voltage with lower magnitude and same polarity with respect to the input voltage. Their operation is based on the principle of resistive voltage division as shown in Figure 2.2 (a). Variable resistor

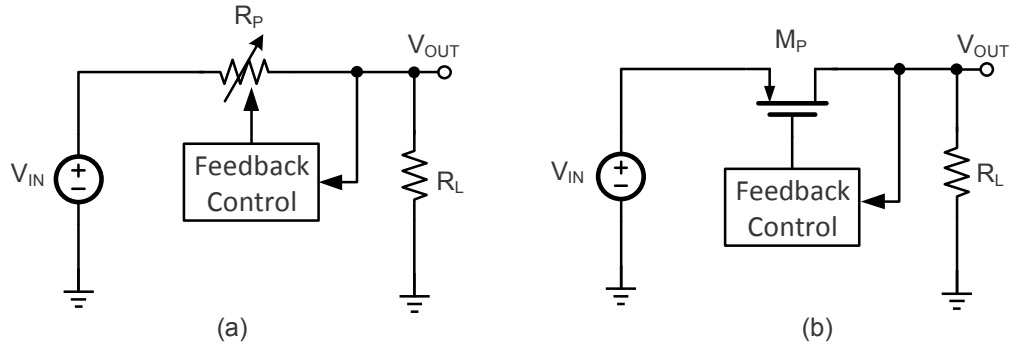


Figure 2.2: Linear voltage regulator block diagram (a) conceptual (b) pass element implementation.

R_P forms a resistor divider with load resistor R_L , which is adjusted via feedback to maintain a constant output voltage V_{OUT} , despite input voltage V_{IN} and/or load variations. From Figure 2.2(a), V_{OUT} can be expressed as,

$$V_{OUT} = \left(\frac{R_L}{R_L + R_P} \right) \cdot V_{IN} \quad (2.1)$$

Neglecting the required current to adjust R_P , the efficiency of the linear voltage regulator can be written as,

$$\eta = \left(\frac{V_{OUT}}{V_{IN}} \right) \cdot 100\% = \left(\frac{R_L}{R_L + R_P} \right) \cdot 100\% \quad (2.2)$$

As can be observed from (2.1) and (2.2), the larger the difference between V_{IN} and V_{OUT} , the smaller the efficiency. For example, if $V_{IN} = 1.8$ V (1.8 V) and $V_{OUT} = 1.6$ V (0.9 V), an efficiency of 89% (50%) is obtained. This is the main disadvantage of linear voltage regulators because for many applications, the value of V_{IN} and V_{OUT} are set by system specifications. Resistor R_P can be implemented with MOS or Bipolar transistors as shown in Figure 2.2(b). Transistor M_P is typically referred to as the pass transistor. In this dissertation, we will limit the discussion to implementations with MOSFETs, and a more detailed discussion will be provided in sections 3 and 4.

2.3.2 Switching-Inductor Converters

Switching-inductor converters combine switches with inductive elements (inductors and/or transformers) to generate a DC output voltage with a different magnitude and/or polarity than the DC input voltage. Switching-inductor voltage regulators can achieve efficiencies above 90% and good voltage regulation. The inductive elements provide energy storage and filtering. They are typically off-chip components due to the limited Q of integrated inductive elements. This increases the overall area and cost of the DC-DC converter with respect to LVRs. Another drawback of switching-inductor voltage regulators are the generation of noise and electromagnetic interference (EMI) [4].

Switching-inductor converters typically operate in closed loop fashion to minimize the effect of load perturbations and/or input voltage variations which could affect the output voltage. Figure 2.3 shows a step-down switching-inductor converter. This

circuit is known as buck converter and it generates an output voltage V_{OUT} smaller than the input voltage V_{IN} . This circuit operates as follows: voltage V_{OUT} is fed back to the controller and compared with the reference voltage V_{REF} . Then, the controller generates a pulse width modulated signal at a given switching frequency (f_s) to turn on/off switches M_P and M_N . Finally, inductor L and capacitor C form a 2^{nd} order LPF to obtain the DC component of signal V_{SW} and generate V_{OUT} . More details on switching-inductor converters will be provided in sections 5 and 6.

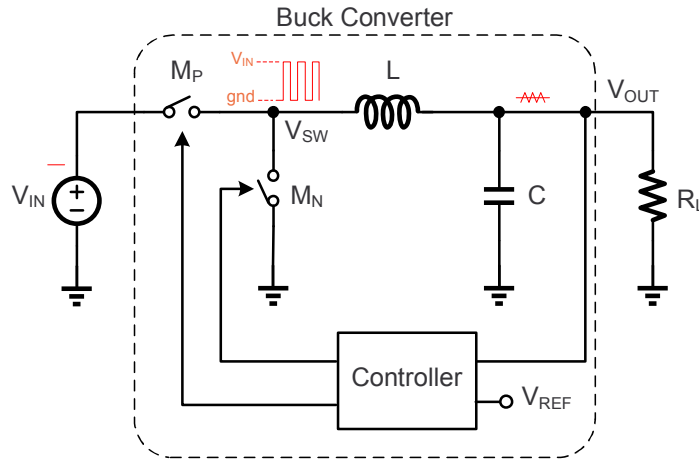


Figure 2.3: Simplified buck converter implementation.

2.3.3 Switching Capacitor Converters

Switched capacitor converters, also known as charge pumps, combine switches and capacitors to generate a lower or higher DC output voltage than the DC input voltage. They can also invert the voltage's polarity. Typical peak efficiencies up to 90 % can be achieved in commercial switched-capacitor converters [5]-[6] for load currents below 300 mA. On-chip switched capacitor voltage regulators can be used

to provide power to non-volatile memory circuits, dynamic random access memories (DRAMs), and analog portions of mixed-signal circuits [2].

A simplified switched capacitor converter implementation is shown in Figure 2.4. The voltage converter generates ideally $V_{OUT} = 2V_{IN}$. Switches S_1 and S_3 are con-

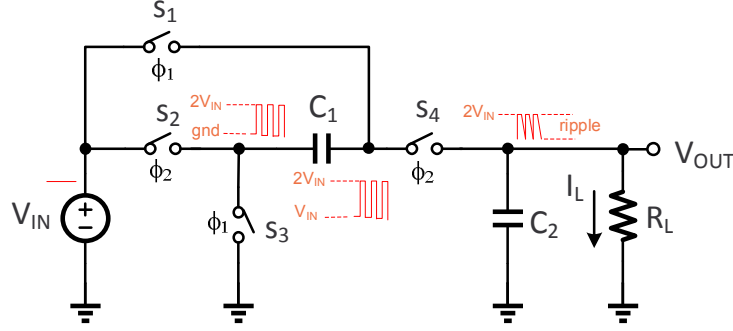


Figure 2.4: Simplified switched capacitor voltage regulator implementation ($V_{OUT} = 2V_{IN}$).

trolled by ϕ_1 control signal, and switches S_2 and S_4 are controlled by ϕ_2 control signal. Control signals ϕ_1 and ϕ_2 do not overlap. When ϕ_1 is high, switches S_1 and S_3 are closed, and switches S_2 and S_4 are open; as a result capacitor C_1 is charged to V_{IN} . In this phase, the load current I_L is supplied through capacitor C_2 . When ϕ_2 is high, switches S_1 and S_3 are open, and switches S_2 and S_4 are closed; hence, capacitor C_2 is charged to $2V_{IN}$. In practice, $V_{OUT} < 2V_{IN}$ due to the voltage drop across the on-resistance of the switches [2].

The main drawback of switched capacitor voltage regulators is their poor load regulation. Load regulation is defined as the output voltage variation due to load current changes. A feedback network [2] can be added to control the conductance of the switches to improve the load regulation. However, this strategy often degrades

the efficiency due to the quiescent current required by the feedback circuit [2].

2.3.4 DC-DC Converters Comparison

Table 2.1 summarizes and compares the main characteristics of the three main types of DC-DC converters. As can be seen, each topology has its own advantages

Table 2.1: DC-DC converters comparison

Parameter	Linear	Switched-inductor	Switched-capacitor
Efficiency	Low	High	High
Voltage conversion	Step down	Step down/up	Step down/up
Output voltage polarity	Same	Different	Different
Area	Small	Large	Medium
Voltage regulation	Good	Good	Poor
Noise	Low	High	High
Current Rating	Low	High	Low

and disadvantages. The selection of one topology over the other is application dependent. Nevertheless, in portable applications the coexistence of both linear and switching regulators is required since both accuracy and efficiency are necessary [7]. In these systems, a stable noise free voltage regulator is required to supply power to noise sensitive circuits. A typical system is shown in Figure 2.5. A switching

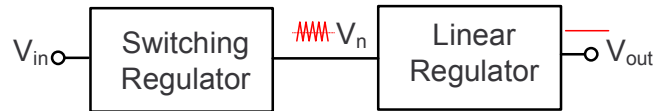


Figure 2.5: Example of a power management system for portable applications.

converter steps down the input voltage to a lower voltage level but noisy (e.g., V_n).

Then a linear voltage regulator generates a low noise output voltage V_{out} from the noisy voltage V_n . The purpose [7]-[8] of the switching is to step down the input voltage in a more efficient way than the linear regulator; while the linear regulator's purpose is to filter the noise and generate a noise free supply voltage.

3. LOW DROP-OUT VOLTAGE REGULATORS *

3.1 Introduction

Low drop-out (LDO) voltage regulators are linear voltage regulators with a drop-out voltage below 600 mV [7], typically in the value of 200 mV. LDO voltage regulators can be classified into two main groups: externally and internally compensated. Moreover, each group can be implemented with an N-type or P-type pass device.

This section discusses design specifications and different types of LDO voltage regulators. In addition, guidelines for measuring voltage regulators and practical design considerations are introduced. Finally, a simple design procedure for a LDO voltage regulator is provided.

3.2 Basic Analysis

Before discussing the non-idealities of the LDO voltage regulator, ideal components will be considered to introduce the basic concept. Figures 3.1 (a) and (b) show the basic LDO architecture and small signal representation, respectively. Applying Kirchhoff's Current Law (KCL) at V_{OUT} and V_{FB} , the output voltage is found to be:

$$V_{OUT} = \frac{g_{mp}A_{EA}V_{REF} + \frac{1+g_{mp}r_{dsp}}{r_{dsp}}V_{IN}}{\frac{1}{r_{dsp}} + \frac{1}{R_L} + \frac{1}{R_{F1}} - \frac{R_{F2}}{R_1(R_{F1}+R_{F2})} + \frac{R_{F2}}{R_{F1}+R_{F2}}g_{mp}A_{EA}} \quad (3.1)$$

where

$$\beta = \frac{R_{F2}}{R_{F2} + R_{F1}}$$

*Part of this section is reprinted with permission from "Low Drop-Out Voltage Regulators: Capacitor-Less Architecture Comparison" by J. Torres et al., accepted for future publication in *IEEE Circuits and Systems Magazine*.

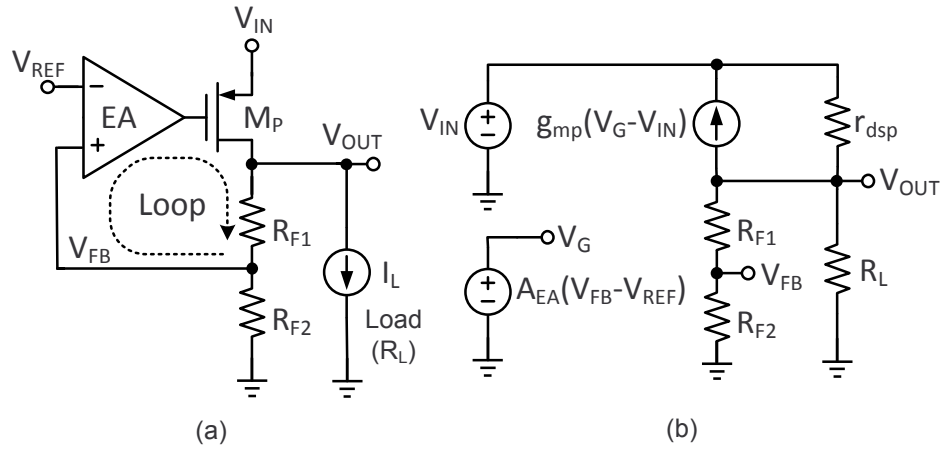


Figure 3.1: (a) Basic LDO voltage regulator topology (b) small signal representation.

Assuming that the term $\beta g_{mp} A_{EA}$ dominates over the other terms in the denominator (this is typically the case in a well designed LDO voltage regulator) and $1 \ll g_{mp} r_{dsp}$, (3.1) simplifies to:

$$V_{OUT} \cong \frac{V_{REF}}{\beta} + \frac{V_{IN}}{\beta A_{EA}} \quad (3.2)$$

Observe that V_{IN} is attenuate by βA_{EA} , and V_{REF} is not. This shows that V_{OUT} is a scale version of V_{REF} , and if βA_{EA} is large enough, it has little dependency on V_{IN} .

3.3 Design Specifications

Key design considerations for LDO voltage regulators include: stability, line/load regulation, line/load transient, power supply rejection (PSR), noise, quiescent current, drop-out voltage, and efficiency. Trade-offs for these parameters are often topology dependent. Definitions for these performance parameters can be found in Appendix A. A brief introduction to these design considerations is presented in this section.

3.3.1 Stability

An LDO voltage regulator is a closed loop feedback system as shown in Figure 3.2. It consists of an error amplifier (EA), pass transistor (M_P), feedback resistors (R_{F1} , R_{F2}), and load capacitor C_L . Capacitors $C_1 = C_{gs} + C_{gb}$ and $C_2 = C_{gd}$, where C_{gb} , C_{gd} , and C_{gs} are the pass transistor parasitic capacitances. Current source I_L represents the load. The stability of the system can be verified by breaking the loop as shown in Figure 3.2 and obtaining the Bode plot. The LDO voltage regulator loop must achieve positive phase margin at the unity gain frequency (UGF) to be stable. To achieve good transient response and minimize ringing, a phase margin greater than 45° is often recommended. I_L may vary several orders of magnitude (i.e., $100\ \mu\text{A}$ to $50\ \text{mA}$) in LDO voltage regulators. This makes the LDO voltage regulator stability analysis more complicated than in a typical amplifier.

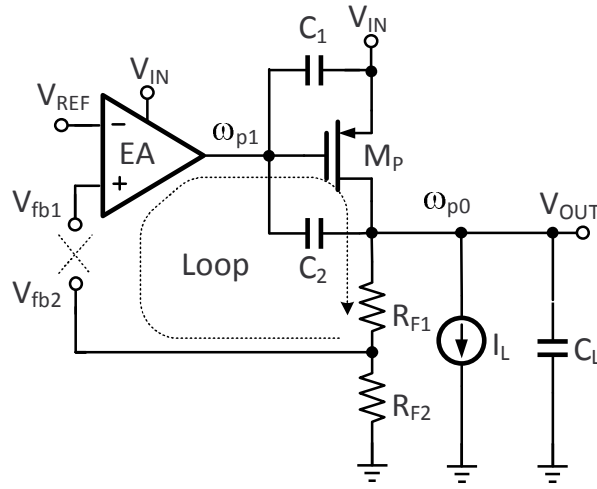


Figure 3.2: LDO voltage regulator setup for stability analysis.

3.3.2 Load Transient

The load transient quantifies the peak output-voltage excursion and signal settling time when the load current is stepped. An LDO regulator with good load-transient response must achieve minimal overshoot/undershoot voltage and fast settling time [9]. The load transient simulation setup is shown in Figure 3.3.

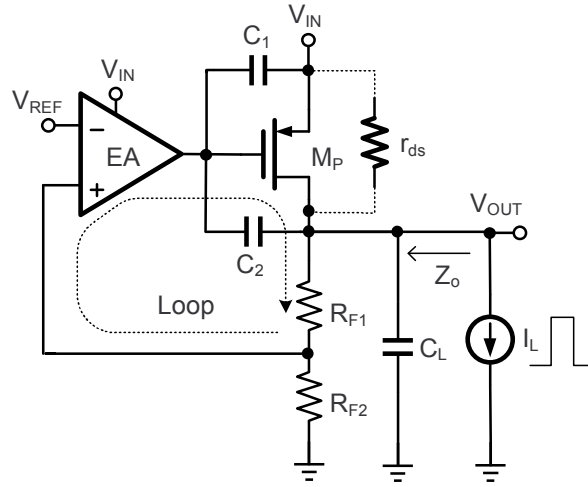


Figure 3.3: Load transient simulation setup.

3.3.3 Load Regulation

The load regulation also quantifies the voltage variation at the output when change in the load current happens, but it is measured once the output voltage is in steady state:

$$\text{Load Regulation} \triangleq \left. \frac{\Delta V_{OUT}}{\Delta I_L} \right|_{t \rightarrow \infty} \quad (3.3)$$

Hence, the load regulation is related to the closed loop DC output resistance of the LDO $R_{out,cl}$ (see Figure 3.3):

$$\Delta V_{out} = \Delta I_L \cdot R_{out,cl} \quad (3.4)$$

where

$$R_{out,cl} = Z_o(s)|_{s=0} = \frac{R_{out}}{1 + \beta g_{mp} R_{out} A_{EA,o}} \cong \frac{1}{\beta g_{mp} A_{EA,o}}. \quad (3.5)$$

where g_{mp} , β , and $A_{EA,o}$ represent the transconductance of the pass transistor, the feedback factor $R_{F2}/(R_{F1} + R_{F2})$, and the EA DC gain, respectively. The open loop resistance R_{out} is equal to the parallel combination of the pass transistor's output resistance (r_{dsp}), load resistance (R_L), and feedback resistors ($R_{F1} + R_{F2}$). As seen in (3.5), the higher $A_{EA,o}$ becomes, the smaller $R_{out,cl}$ becomes resulting in better load regulation. $A_{EA,o}$ at the maximum load current $I_{L,max}$ is particularly necessary to achieve good load regulation. Parasitic resistances (e.g., due to PCB trace, bonding wire, etc.) and systematic input-offset voltages can degrade the load regulation performance even further [7]. Figure 3.4 shows a simplified block diagram of an LDO voltage regulator including the equivalent PCB trace resistance (R_{Trace}) and inductance (L_{Trace}), and equivalent bonding wire resistance (R_B) and inductance (L_B) [7]. The purpose of the Kelvin connection will be explained later in section 3.9.1.2.

3.3.4 Power Supply Rejection (PSR)

Before discussing in detail power supply rejection in LDO voltage regulators, the difference between power supply rejection ratio ($PSRR$) in amplifiers and power supply rejection (PSR) in LDO voltage regulators will be clarified since both terms are often confused with each other. A general conceptual block diagram depicted in Figure 3.5(a) shows the transfer functions from the power supply (V_{DD}) and input

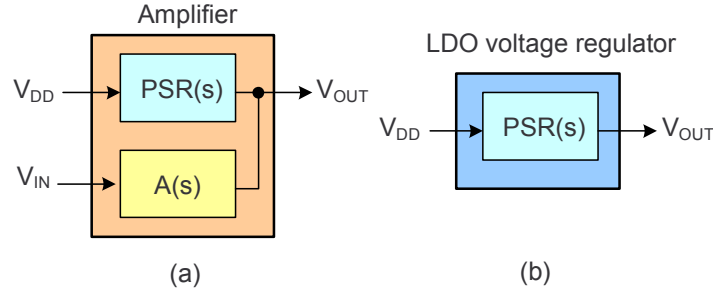


Figure 3.5: General conceptual block diagrams for (a) an amplifier (b) LDO voltage regulator.

from the ripple at the input. The finite PSR in LDO regulators is due to several paths between the input and output. Figure 3.6 shows four paths that could couple input-voltage ripple to the LDO regulator output [10]. The ripple coming from

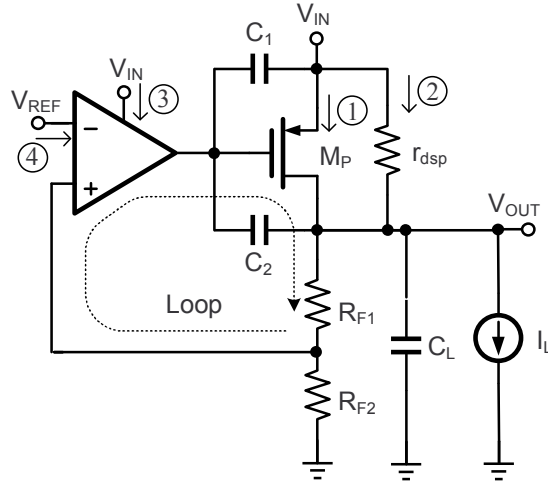


Figure 3.6: Input-to-output ripple paths in LDO regulators [10].

path 4 (voltage reference) is minimum when a high PSR voltage reference [10] is implemented. Otherwise, it can be reduced by adding a low-pass filter to the output

of the voltage reference at the expense of increasing PCB area [11]. Therefore, the ripple contribution due to path 4 is neglected. Regarding path 3, the PSR transfer function of the LDO regulator strongly depends on the type of error amplifier [12] and the type of device used as pass element. The concept of the Type-A and Type-B error amplifiers was introduced in [12] to analyze the PSR of CL-LDO regulators. It can be shown that the PSR of Type-A and Type-B EAs are approximately 1 or 0, respectively. Figures 3.7(a) and (b) show the Type-A small-signal model for PSR analysis and an example of Type-A EA, respectively. Figures 3.8(a) and (b)

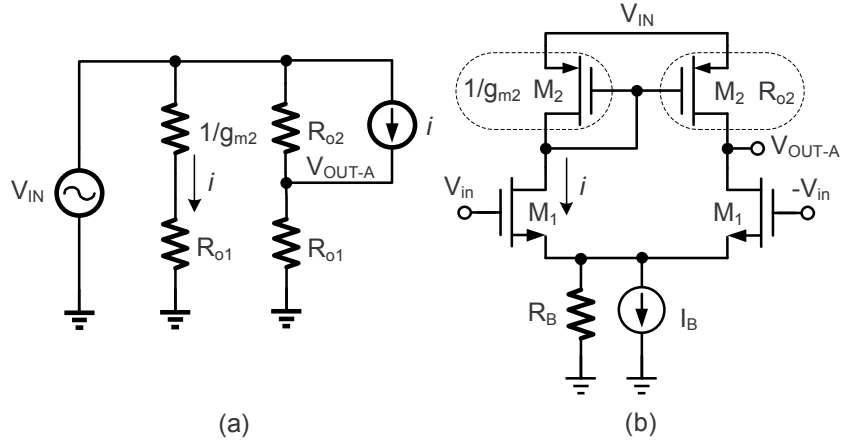


Figure 3.7: (a) Small signal model for PSR of Type-A amplifiers and (b) transistor level example of Type-A amplifier [12].

show the Type-B small-signal model for PSR analysis and an example of Type-B EA, respectively [12]. Current i is approximately V_{IN}/R_{o1} for $R_{o1} \gg 1/g_{m2}$, where $R_{o1} \cong 1/g_{m1} + 2R_B$. Resistor R_B represents the current source I_B small signal resistance. Table 3.1 classifies some common amplifier topologies in Type-A and Type-B amplifiers. PSR analysis for externally and internally compensated LDO voltage regulators is provided later in this section and will take into account Type-A

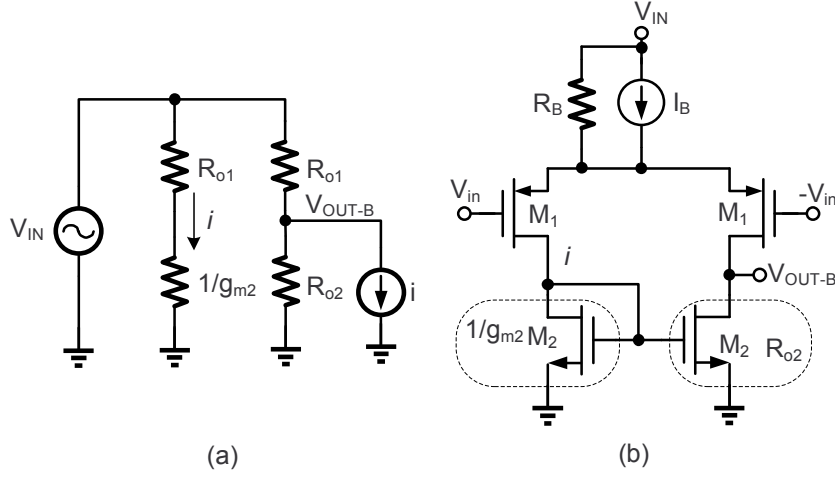


Figure 3.8: (a) Small signal model for PSR of Type-B amplifiers and (b) an example of Type-B error amplifier [12].

and Type-B amplifiers.

3.3.5 Line Transient and Regulation

Line transient measures the output voltage variation in response to a voltage step at the input of the LDO regulator. Line transient is related to PSR, since both quantify the change in V_{OUT} due to a variation in V_{IN} ; however, they differ in that line transient/PSR are large/small-signal parameters, respectively [11]. Nevertheless, improving PSR at low and high frequencies typically improves line regulation and line transient response, respectively. Assuming, for the sake of simplicity, that we can apply small-signal perturbation analysis, then

$$\Delta V_{OUT} = PSR(s) \cdot \Delta V_{IN} \quad (3.8)$$

where $\Delta V_{IN} = V_{step}/s$ in the Laplace domain and $PSR(s)$ is the power supply rejection transfer function of the system. In fact, small changes in V_{IN} would cause

Table 3.1: Type-A and Type-B single stage amplifier characteristics

Topology	Input Stage	Active Load	Amplifier Type
Simple	NMOS DP	PMOS CM	Type-A
	PMOS DP	NMOS CM	Type-B
Telescopic	NMOS DP	PMOS CM	Type-A
	PMOS DP	NMOS CM	Type-B
Folded-Cascode	NMOS/PMOS DP	PMOS CM	Type-A
	NMOS/PMOS DP	NMOS CM	Type-B

* DP = Differential pair and CM = Current mirror.

the parameters of $PSR(s)$ to change, adding nonlinearity to the response. However, we note that the line transient is strongly correlated to the power supply rejection transfer function of the system.

The line regulation also quantifies the voltage variation at the output when change in the input voltage happens, but it is measured once the output voltage is in steady-state:

$$Line\ Regulation \triangleq \left. \frac{\Delta V_{OUT}}{\Delta V_{IN}} \right|_{t \rightarrow \infty} \quad (3.9)$$

Hence, the line regulation is related to the PSR at low-frequencies (DC):

$$Line\ Regulation \cong PSR(s = 0) \quad (3.10)$$

As seen in 3.10, the better the PSR at low frequencies (DC), the better the line regulation. A simple approximation for $PSR(s = 0)$ provides insight as:

$$PSR(s = 0) \geq \left| 20 \cdot \log_{10} \left(\frac{1}{\beta A_{EA,o}} \right) \right| \quad (3.11)$$

3.3.6 Noise

Noise in LDO regulators refers to the thermal and flicker noise in transistors and resistors. It can be specified as output voltage noise spectral density (V/\sqrt{Hz}) or as integrated output noise voltage (V_{rms}), which is essentially the output spectral noise density integrated over a bandwidth [13]-[14]. For instance, if the LDO provides a regulated voltage to a voltage-control oscillator (VCO), the output spectral noise density curve would prove more useful for phase-noise/jitter computation. If instead, the LDO regulated an ADC, then the integrated RMS noise could be more appropriate [14]. Fig. 3.9 shows the main noise contributors in an LDO regulator. $S_{n,ref}(f)$, $S_{n,EA}(f)$, $S_{n,MP}(f)$, $S_{n,R_{F1}}(f)$, and $S_{n,R_{F2}}(f)$ represent the noise power spectral density of the voltage reference, error amplifier, pass transistor, R_{F1} , and R_{F2} , respectively [15].

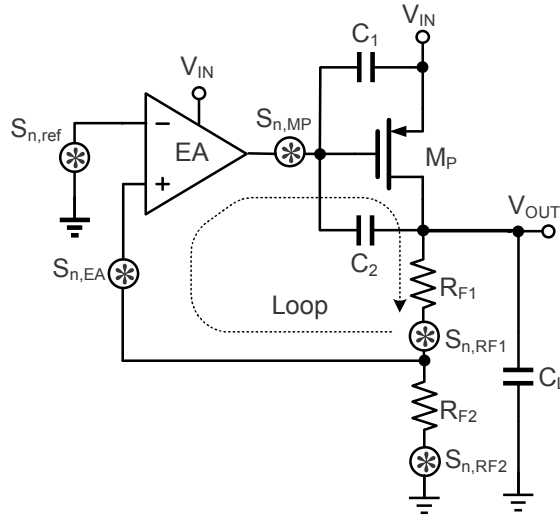


Figure 3.9: LDO regulator's major noise contributors.

The total output noise power spectral density of the LDO regulator is:

$$S_{n,o}(f) = \left(S_{n,ref}(f) + S_{n,EA}(f) + \frac{S_{n,MP}(f)}{A_{EA}^2} \right) \cdot \left(1 + \frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,R_{F2}}(f) \cdot \left(\frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,R_{F1}}(f). \quad (3.12)$$

Notice that the noise contribution of the pass transistor can be neglected since it is divided by the error amplifier loop gain which is typically high. Thus, the total output noise power spectral density can be approximated as:

$$S_{n,o}(f) = (S_{n,ref}(f) + S_{n,EA}(f)) \cdot \left(1 + \frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,R_{F2}}(f) \cdot \left(\frac{R_{F1}}{R_{F2}} \right)^2 + S_{n,R_{F1}}(f). \quad (3.13)$$

The noise coming from the voltage reference can be significantly reduced by adding a low-pass filter [13] to the output of the voltage reference at the expense of increasing PCB area. The error amplifier and feedback resistors noise are typically the dominant sources of a LDO regulator noise. To minimize the error amplifier noise its differential pair transistors dimensions need to be large enough to reduce its flicker noise [15]. Reducing feedback-resistor noise implies smaller resistances, which in turn increases LDO power consumption. LDO voltage regulators with an rms output voltage noise as low as $4.17 \mu V_{rms}$ for a bandwidth from 10 Hz to 100 kHz are currently commercially available [16].

3.3.7 Quiescent Current

Quiescent current is the difference between the input current (I_{IN}) of the LDO voltage regulator and load current [17],

$$I_Q = I_{IN} - I_L \quad (3.14)$$

This current is particularly important at light loads to maximize efficiency. Quiescent current consists of the EA, V_{REF} , and R_{F1}/R_{F2} currents in LDO voltage regulator with a MOS pass transistor.

3.3.8 Drop-Out Voltage

Drop-out voltage is the minimum difference between the input and output voltages at which the circuit ceases to regulate [17]:

$$V_{DO} = \min(V_{IN} - V_{OUT}) \quad (3.15)$$

The drop-out voltage is the condition where minimum power is dissipated in the regulator since this voltage and load current are a large component of the power losses in the system. As a result, low drop-out voltage regulators exhibit better efficiency than high drop-out voltage regulators.

3.3.9 Efficiency

Efficiency (η) is defined as the ratio of the output power P_{OUT} over the input power P_{IN} :

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L V_{OUT}}{(I_L + I_Q) V_{IN}} < \frac{V_{OUT}}{V_{IN}} \quad (3.16)$$

where I_L and I_Q are the load and quiescent currents, respectively. If the quiescent current is much smaller than I_L , the maximum η that can be achieved is V_{OUT}/V_{IN} .

For example, the maximum efficiency for a linear regulator when $V_{IN} = 3.3 \text{ V}$ (3.3 V) and $V_{OUT} = 1.8 \text{ V}$ (3.1 V) is 54.5% (93.9%), respectively. As can be observed, the smaller drop-out voltage, the higher the η .

3.4 Externally Compensated LDO Voltage Regulators

An externally compensated LDO voltage regulator is shown in Figure 3.10. Their

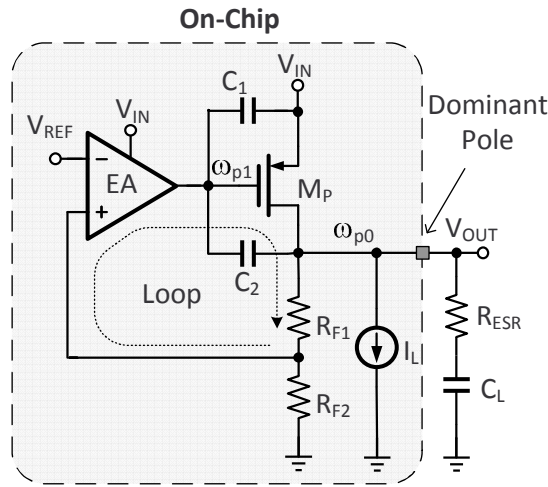


Figure 3.10: Externally compensated LDO voltage regulator with PMOS pass transistor.

dominant pole ω_{po} is located at V_{OUT} . From the stability point of view, it is convenient to use a large output capacitor (C_L) and a p-type pass transistor to achieve a large RC time constant to maintain ω_{po} (g_{dsp}/C_L) dominant over the entire load current range. C_L is typically a bulky off-chip capacitor, and its value is often in the order of several micro-farads. In addition, C_L minimizes the output impedance (Z_{OUT}) at high frequencies; thereby minimizing V_{OUT} voltage variations ($\Delta V_{OUT} = Z_{OUT} \cdot \Delta I_L$) during load transient events. This off-chip capacitor increases the system's cost due to its market value and increases the PCB area. Moreover, it requires

an additional package's pin. Nevertheless, in high power applications due to large I_L variations, their use is inevitable to minimize ΔV_{OUT} [7]. Resistor R_{ESR} represents C_L 's parasitic resistance and/or a resistance added to generate a zero ($1/(R_{ESR}C_L)$) for compensation purposes. Externally compensated LDOs can be implemented with a NMOS pass transistor; however, C_L needs to be extremely large to make ω_{p0} the dominant pole because the open loop resistance of this topology is approximately $1/g_{mn}$, where g_{mn} is the transconductance of the NMOS pass transistor. In many cases, an off-chip C_L is still used but the dominant pole is inside the loop (e.g., ω_{p1}).

3.4.1 Stability

The small signal model for the circuit in Figure 3.10 is shown in Figure 3.11. Parameters g_{me} and R_{oe} represent the error amplifier transconductance and output

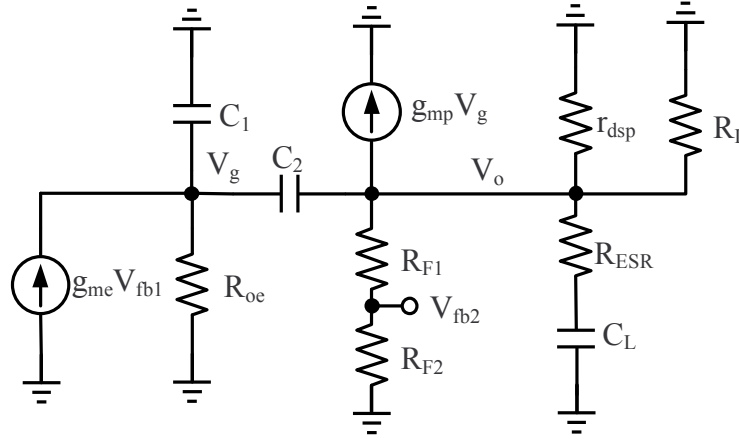


Figure 3.11: Small-signal model for an externally compensated LDO voltage regulator with PMOS pass transistor.

resistance, respectively. Capacitance $C_1 = C_{gs} + C_{gb}$ and capacitance $C_2 = C_{gd}$, where C_{gs} , C_{gb} , and C_{gd} are parasitic capacitances of the pass transistor M_P . The

loop transfer function can be expressed in general as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} = -A_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \cdot \left(1 - \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right) \cdot \left(1 + \frac{s}{\omega_{p3}}\right)} \quad (3.17)$$

where

$$\begin{aligned} g_{mp} &= \sqrt{K_p I_L}, \quad R_{out} = R_L || r_{dsp} || (R_{F1} + R_{F2}) \propto \frac{1}{I_L}, \\ A_{DC} &= \beta g_{me} R_{oe} g_{mp} R_{out} \propto \frac{1}{\sqrt{I_L}}, \quad \beta = \frac{R_{F2}}{R_{F1} + R_{F2}}, \quad \omega_{z1} = \frac{1}{R_{ESR} C_L}, \\ \omega_{z2} &= \frac{g_{mp}}{C_2} \propto \sqrt{I_L}, \quad \omega_{p1} = \frac{1}{R_{out} C_L} \propto I_L, \quad \omega_{p2} = \frac{1}{R_{oe} (C_2 + C_1)}, \\ \omega_{p3} &= \frac{C_1 + C_2}{C_1 C_2 R_{ESR}}, \quad UGF \cong \frac{\beta g_{me} R_{oe} g_{mp}}{C_L} \propto \sqrt{I_L} \end{aligned}$$

Observe that the unity gain frequency (UGF) is approximately a function of $\sqrt{I_L}$. Figure 3.12 shows the Bode plot for the externally compensated LDO with a PMOS pass transistor. As can be seen, the location of UGF varies as I_L changes. Note that the worst-case stability condition occurs at $I_{L,max}$.

3.4.2 Load Transient

In the case of the externally compensated LDO regulators, the maximum output voltage variation ΔV_{OUT} can be estimated using the equivalent circuit shown in Figure 3.13. In Figure 3.13, it is assumed that the feedback loop does not react fast enough to a sudden load change; as a result, the output impedance is determined by the output capacitor. Hence, the maximum ΔV_{OUT} is given by:

$$\Delta V_{OUT} = \frac{\Delta I_L \cdot \Delta t_1}{C_L} + R_{ESR} \cdot \Delta I_L \quad (3.18)$$

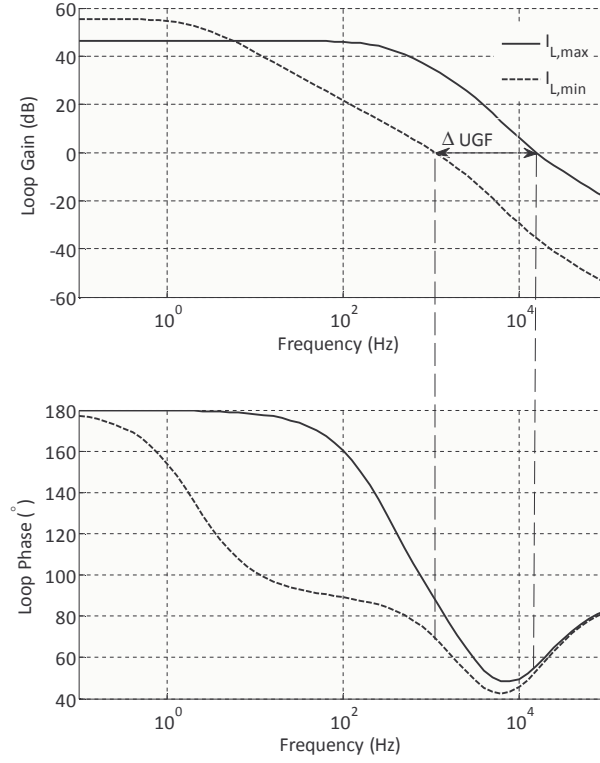


Figure 3.12: Externally compensated LDO voltage regulator with PMOS pass transistor Bode plot.

where C_L is the load capacitance, ΔI_L is the load current step, and Δt_1 is the time that the loop takes to react. Δt_1 is a function of the closed-loop bandwidth and the slew rate associated with the capacitance at the gate of the pass transistor and can be approximated by [9], [15]:

$$\Delta t_1 \cong \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + \frac{\Delta V}{I_{sr}} C_p \quad (3.19)$$

Thus,

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{C_L} \cdot \left(\frac{1}{BW_{cl}} + \frac{\Delta V}{I_{sr}} C_p \right) + R_{ESR} \cdot \Delta I_L \quad (3.20)$$

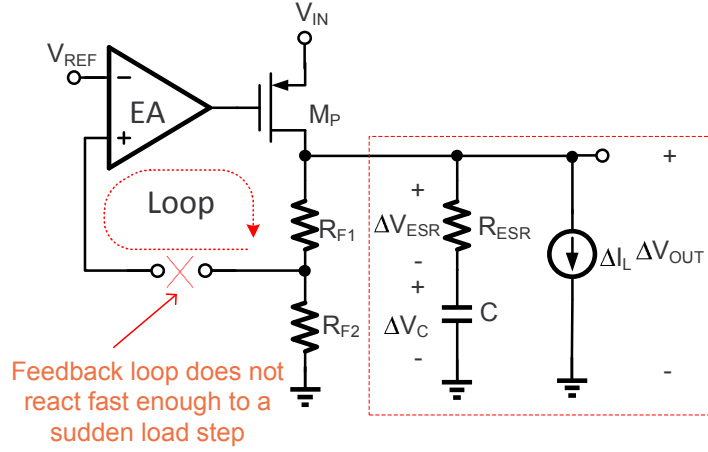


Figure 3.13: Equivalent circuit for load transient analysis.

where t_{sr} and I_{sr} are the slew rate time and the available current of the amplifier to drive the pass transistor, respectively. Parameter BW_{cl} is the closed-loop bandwidth of the system which is equivalent to the unity gain frequency (UGF); whereas C_p and ΔV are the capacitance and voltage variation at the gate of the pass transistor, correspondingly.

As it can be observed from (3.20), the output voltage variation during load transients is inversely proportional to C_L . Capacitor C_L is typically an off-chip capacitor in the order of microfarads to achieve good load transient performance. It is clear that to achieve certain transient performance, the loop bandwidth and the slew rate at the gate of the pass transistor need to be optimized. This typically translates into higher quiescent current. Moreover, R_{ESR} needs to be minimized for large load steps to reduce the voltage dips/surges.

3.4.3 Power Supply Rejection

Figures 3.14 and 3.15 show the PSR small signal model for externally compensated LDOs with PMOS pass transistor as well as Type-A and Type-B EAs, respec-

tively. These small signal models are based on Figure 3.10. Applying Kirchhoff's

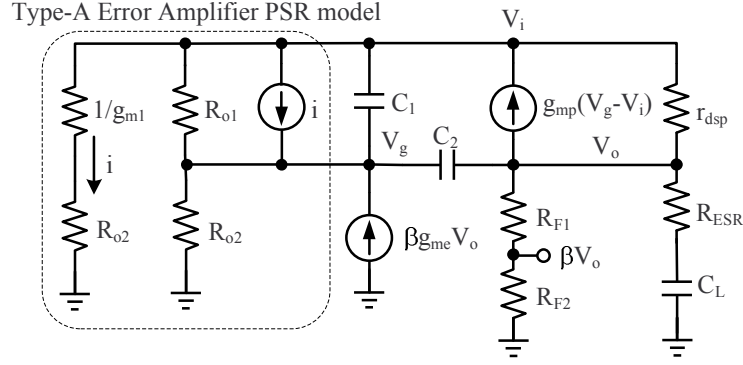


Figure 3.14: PSR small signal model for externally compensated LDO voltage regulator with PMOS pass transistor and Type-A EA.

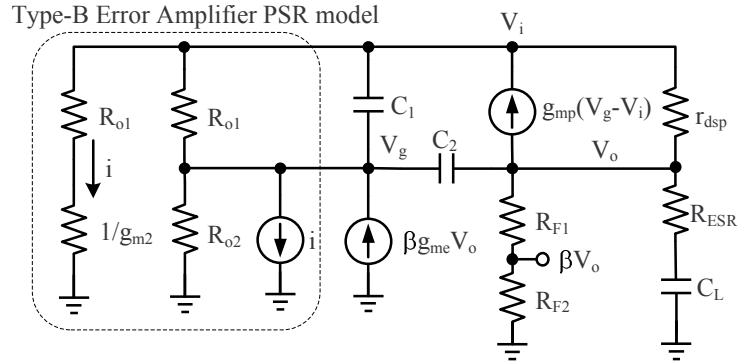


Figure 3.15: PSR small signal model for externally compensated LDO voltage regulator with PMOS pass transistor and Type-B EA.

current law (KCL) at nodes V_g and V_o in Figures 3.14 and 3.15, we obtain the following:

$$\frac{V_o(s)}{V_i(s)} = PSR_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{z1,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{z2,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{z3,psr}}\right)}{\left(1 + \frac{s}{\omega_{p1,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{p2,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{p3,psr}}\right)} \quad (3.21)$$

where

$$PSR_{DC} \cong \frac{1 + g_{mp}r_{dsp}(1 - A_{PSR})}{\beta g_{mp}r_{dsp}g_{me}R_{oe}}, \quad \omega_{z2,psr} = \frac{1}{R_{ESR}C_L}, \quad \omega_{z3,psr} = \frac{g_{mp}}{C_1},$$

$$\omega_{p1,psr} = \frac{1}{R_{ESR}C_L}, \quad \omega_{p2,psr} = \frac{\beta g_{me}g_{mp}R_{ESR}}{C_1 + 2C_2}, \quad \omega_{p3,psr} = \frac{C_1 + C_2}{C_1C_2R_{ESR}}$$

In (3.21), it was assumed $\beta g_{mp}r_{dsp}g_{me}R_{oe}C_LR_{ESR} \gg C_Lr_{dsp}$. At light loads ($I_{L,min}$), this assumption may not hold true as $\beta g_{mp}r_{dsp}g_{me}R_{oe}C_LR_{ESR} \ll C_Lr_{dsp}$; hence,

$$\omega_{p1,psr} = \frac{\beta g_{mp}g_{me}R_{oe}}{C_L}, \quad \omega_{p2,psr} = \frac{1}{(C_1 + 2C_2)R_{oe}} \quad (3.22)$$

Table 3.2 shows the analytical expressions for $\omega_{z1,psr}$ and $|PSR|_{DC}$ for an externally compensated LDO voltage regulator implemented with Type-A and Type-B error amplifiers. As can be seen from Table 3.2, the LDO voltage regulator implemented with Type-A amplifier presents a higher DC PSR than the one implemented with Type-B amplifier for the same loop gain.

Table 3.2: Analytical expressions for PSR of an externally compensated LDO voltage regulator

Error Amplifier	A_{PSR}	$\omega_{Z1,psr}$	$ PSR _{DC}$
<i>Type – A</i>	1	$1/(g_{mp}r_{dsp}C_2R_{oe})$	$\frac{1}{\beta g_{me}R_{oe}g_{mp}r_{dsp}}$
<i>Type – B</i>	0	$1/(R_{oe}C_2)$	$\frac{1}{\beta g_{me}R_{oe}}$

3.5 Internally Compensated LDO Voltage Regulators

An internally compensated LDO voltage regulator, also known as a capacitor-less (CL-LDO) or capacitor-free LDO voltage regulator [18], is shown in Figure 3.16.

Their dominant pole ω_{p1} is inside the loop to take advantage of the high output resistance of the error amplifier and avoid the need of a large compensation capacitor.

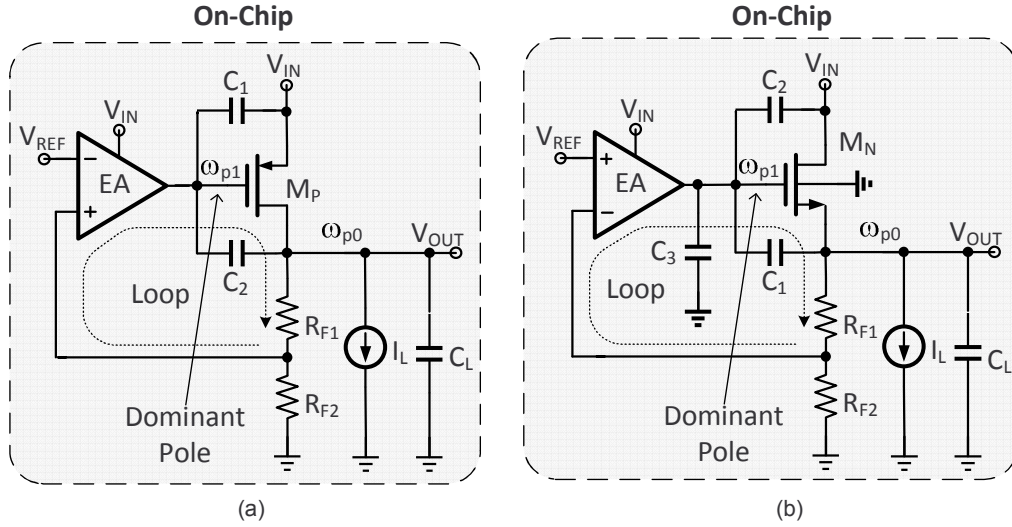


Figure 3.16: Internally compensated LDO voltage regulator with (a) PMOS and (b) NMOS pass transistors.

They can be implemented with either P-type or N-type pass transistors as shown in Figures 3.16 (a) and (b), respectively. In Figure 3.16, C_L models the parasitic capacitors and/or any integrated capacitor at the output node. Capacitor C_L is typically in the order of pico-farads in CL-LDO voltage regulators.

3.5.1 Stability

There are many CL-LDO topologies with multi-stage EAs and multiple feedback loops. Many of those topologies will be discussed in Section 4. Here the discussion is limited to CL-LDOs with one stage EA and one active feedback loop.

3.5.1.1 PMOS pass transistor

The small signal model for a Miller-compensated CL-LDO voltage regulator (Figure 3.16 (a)) is shown in Figure 3.17. Capacitance $C_2 = C_{gd} + C_m$, where C_m is

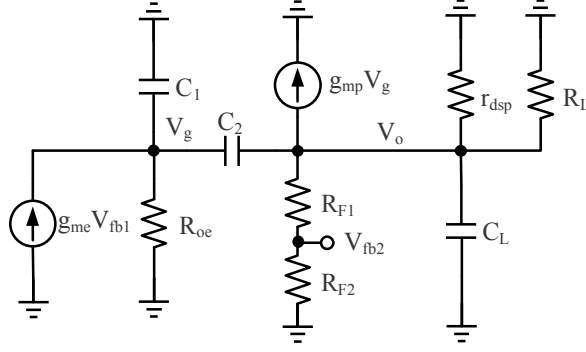


Figure 3.17: Small signal model for internally compensated LDO voltage regulator with PMOS pass transistor.

a compensation capacitance. The loop transfer function can be expressed in general as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} = A_{DC} \cdot \frac{\left(1 - \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (3.23)$$

where

$$A_{DC} = \beta g_{me} R_{oe} g_{mp} R_{out} \propto \frac{1}{\sqrt{I_L}}, \quad \beta = \frac{R_{F2}}{R_{F1} + R_{F2}}, \quad \omega_{z1} = \frac{g_{mp}}{C_2} \propto \sqrt{I_L},$$

$$\omega_{p1} \cong \frac{1}{((1 + g_{mp} R_{out}) C_2 + C_1) R_{oe}}, \quad \omega_{p2} \cong \frac{g_{mp}}{C_L \left(1 + \frac{C_1}{C_2}\right) + C_1} \propto \sqrt{I_L},$$

$$UGF \cong \frac{\beta g_{me} R_{oe} g_{mp} R_{out}}{((1 + g_{mp} R_{out}) C_2 + C_1) R_{oe}}$$

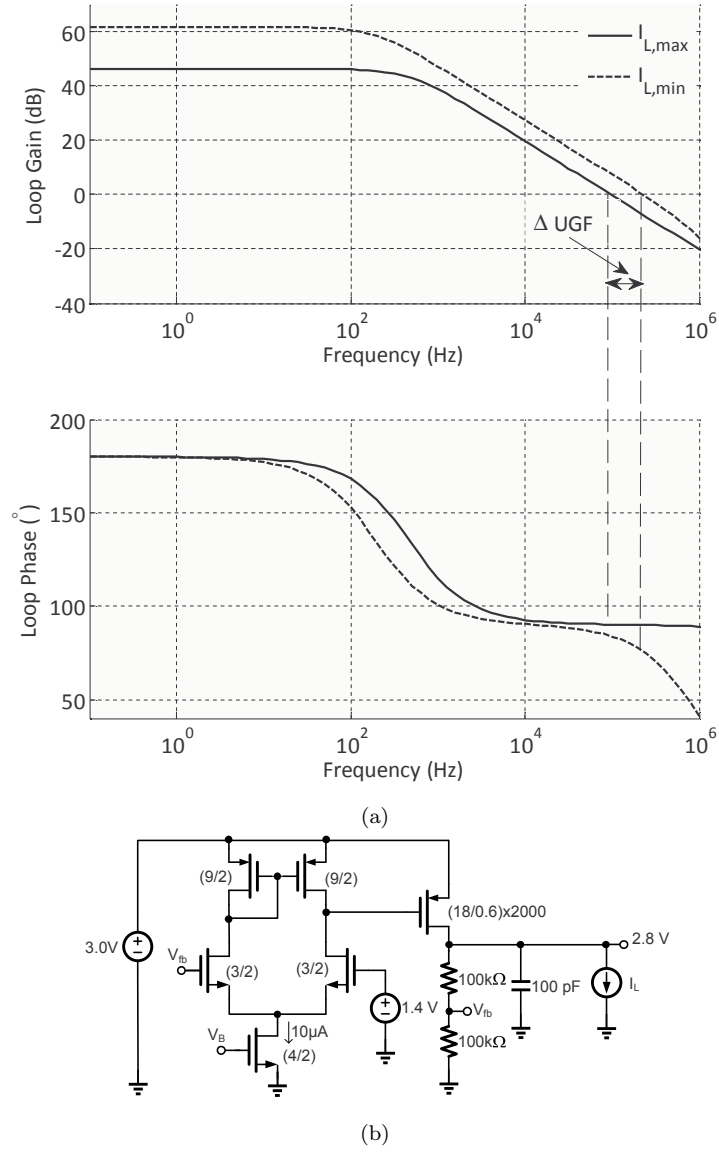


Figure 3.18: (a) Internally compensated LDO voltage regulator with PMOS pass transistor Bode plot (b) schematic utilized to obtain (a).

Figure 3.18(a) shows the Bode plot for an internally compensated LDO with PMOS pass transistor for $I_{L,min} = 100 \mu\text{A}$ and $I_{L,max} = 50 \text{ mA}$. These results were obtained using the schematic shown in Figure 3.18(b) for $0.5 \mu\text{m}$ CMOS technology. As can be seen, the location of UGF varies as I_L changes. Note that unlike externally compensated LDO regulators with a PMOS pass transistor where the worst-case stability condition occurs at $I_{L,max}$, the worst-case stability for an internally-compensated LDO regulator with a PMOS pass transistor occurs at $I_{L,min}$ because UGF increases, and ω_{p2} and ω_{z1} decrease.

3.5.1.2 NMOS Pass Transistor

The small signal model for the circuit in Figure 3.16 (b) is shown in Figure 3.19. Parameters g_{mn} , g_{mb} , and r_{dsn} represent the transconductance, body transconductance, and output resistance of the NMOS pass transistor, respectively.

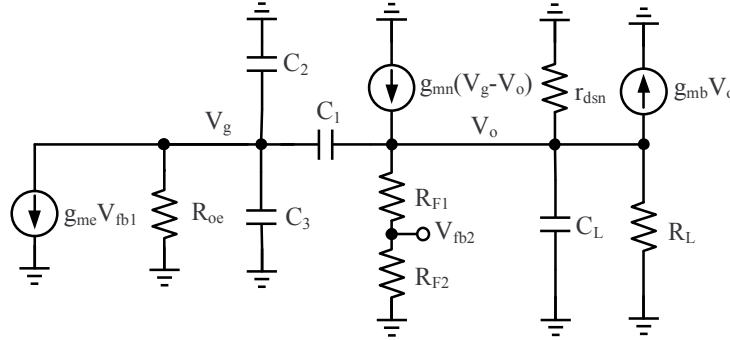


Figure 3.19: Small signal model for internally compensated LDO voltage regulator with NMOS pass transistor.

tance (not included in the P-Type case since the bulk is connected to the source), and output resistance of the NMOS pass transistor, respectively. Capacitances $C_1 = C_{gs}$, $C_2 = C_{gd}$, and $C_3 = C_{gb} + C_m$, where C_{gb} , C_{gd} , C_{gs} are parasitic capacitances of the NMOS pass transistor, and C_m is a compensation capacitance. The open loop

transfer function can be expressed in general as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} = A_{DC} \cdot \frac{(1 + \frac{s}{\omega_{z1}})}{(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}})} \quad (3.24)$$

where

$$A_{DC} \cong \beta g_{me} R_{oe} \cdot \frac{g_{mn}}{g_{mn} + g_{mb}}, \quad \beta = \frac{R_{F2}}{R_{F1} + R_{F2}}, \quad \omega_{z1} = \frac{g_{mn}}{C_1} \propto \sqrt{I_L},$$

$$\omega_{p1} \cong \frac{1}{R_{oe}(C_2 + C_3)}, \quad \omega_{p2} \cong \frac{g_{mn} + g_{mb}}{C_L \left(1 + \frac{C_1}{C_2 + C_3}\right) + C_1} \propto \sqrt{I_L}$$

$$UGF \cong \frac{\beta g_{me}}{C_2 + C_1} \cdot \frac{g_{mn}}{g_{mn} + g_{mb}}$$

Figure 3.20 (a) shows the Bode plot for an internally compensated LDO with NMOS pass transistor for $I_{L,min} = 100 \mu\text{A}$ and $I_{L,max} = 50 \text{ mA}$. These results were obtained using the schematic shown in Figure 3.20 (b) for $0.5 \mu\text{m}$ CMOS technology. The 2V voltage source was utilized to emulate the effect of the charge such that the voltage at the gate of the pass transistor can go above V_{IN} (i.e., 3V) for large I_L (i.e., 50 mA). As can be seen, the UGF varies as I_L changes. This is due to the gain variation of the pass transistor with I_L . Moreover, it can be observed that the worst-case stability scenario for an internally-compensated LDO regulator with NMOS pass transistor occurs at $I_{L,min}$ because UGF increases, and ω_{p2} and ω_{z1} decreases.

3.5.2 Load Transient

For small load steps, the undershoot/overshoot of the output voltage is proportional to the output impedance $Z_o(s)$ (see Figure 3.3). The CL-LDO regulator has

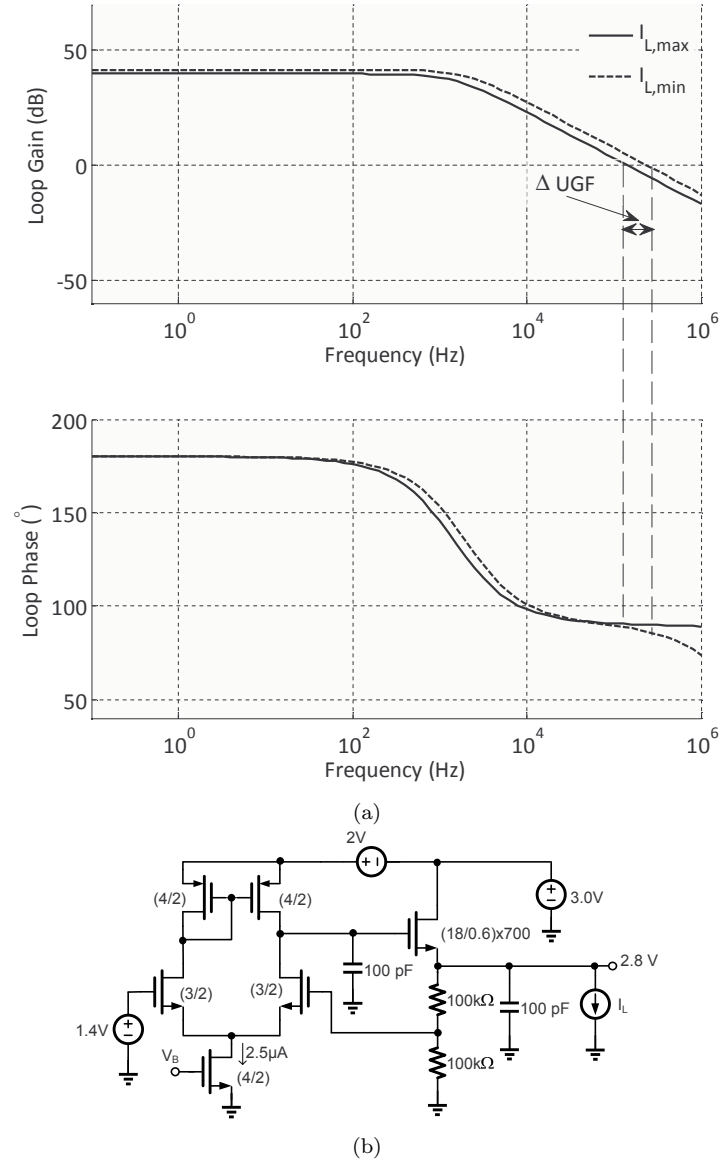


Figure 3.20: (a) Internally compensated LDO voltage regulator with NMOS pass transistor Bode plot and (b) schematic utilized to obtain (a).

small-signal output impedance given by:

$$Z_o(s) = \frac{V_{OUT}(s)}{I_L(s)} \approx \frac{R_{out}}{1 + \beta g_{me} R_{oe} g_{mp} R_{out}} \cdot \frac{1 + s(C_2 + C_1)R_{oe}}{s^2 \frac{C_L(C_2 + C_1) + C_2 C_1}{\beta g_{me} g_{mp}} + s \frac{C_2}{\beta g_{me}} + 1} \quad (3.25)$$

where g_{me} and R_{oe} denote the error-amplifier transconductance and output resistance, respectively, and $R_{out} = r_{dsp} || (R_{F1} + R_{F2})$. In (3.25), it is assumed that $\beta g_{me} \ll g_{mp}$. Assuming, for simplicity, that we can apply small-signal perturbation analysis, then

$$\Delta V_{OUT} = Z_o(s) \cdot \Delta I_L \quad (3.26)$$

where $\Delta I_L = I_{step}/s$ is in the Laplace domain. In fact, small variations in I_L would cause the parameters of $Z_o(s)$ to change, adding nonlinearity to the response. However, we note that the load transient is strongly correlated to the output impedance. While externally compensated regulators' $Z_o(s)$ is dominated by a microfarad-range load capacitor, CL-LDOs $Z_o(s)$ arises chiefly from the open loop gain and can be improved by increasing loop bandwidth. Table 3.3 compares the output impedance of externally and internally compensated LDO voltage regulators.

Table 3.3: Externally versus internally compensated LDO voltage regulators output impedance comparison

Z_o	Externally Compensated	Internally Compensated
Low-frequencies	$\cong 1/(\beta g_{mp} g_{me} R_{oe})$	$\cong 1/(\beta g_{mp} g_{me} R_{oe})$
Medium-to-high frequencies	Dominated by C_L , minimum value is limited by R_{ESR}	Determine by the loop transfer function

For large load current steps, the analysis is particularly challenging since the pass transistor operates in three different operating regions (E.g. subthreshold, saturation,

and triode regions) over the entire load current range. In addition, the transconductance, conductance, and parasitic capacitors of the pass transistor vary dynamically with the load current, thereby complicating the analysis even further. Figure 3.21 shows an illustrative example of how the CL-LDO output impedance varies as the load current changes and how the pass transistor operates in different regions over the entire load current range. Figure 3.22 depicts the parasitic capacitance of the

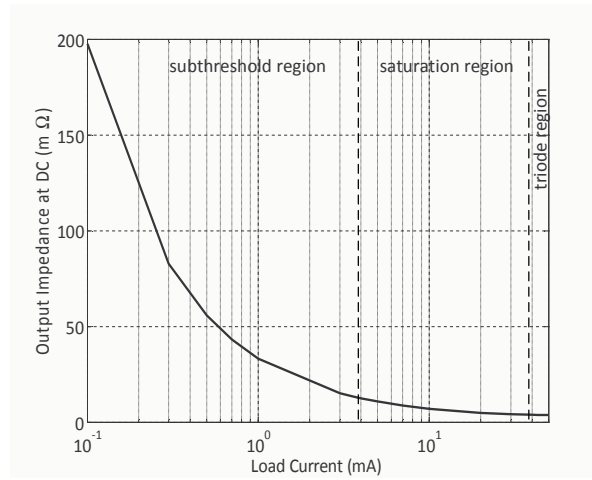


Figure 3.21: Output impedance at DC versus load current.

pass transistor variation versus load current. As can be seen, the CL-LDO output impedance and the parasitic capacitances of the pass transistor significantly vary over the entire current range. Fortunately, it has been observed that improving the slew rate (a large signal parameter) helps to minimize the undershoots/overshoots during large load current steps. In CL-LDO regulators, the slew rate (I_{bias}/C_{gate}) is highly dependent on total capacitance at the gate of the pass transistor and the bias current of the EA's stage driving it. Figure 3.23 shows an example of how the V_{out} undershoot amplitude varies versus the bias current of the EA's output stage. As

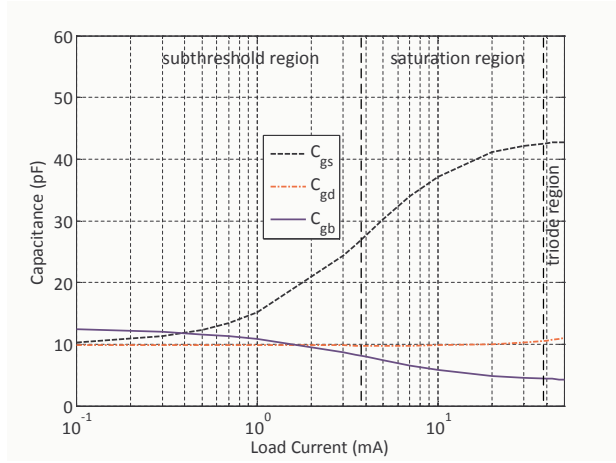


Figure 3.22: M_P parasitic capacitance versus load current.

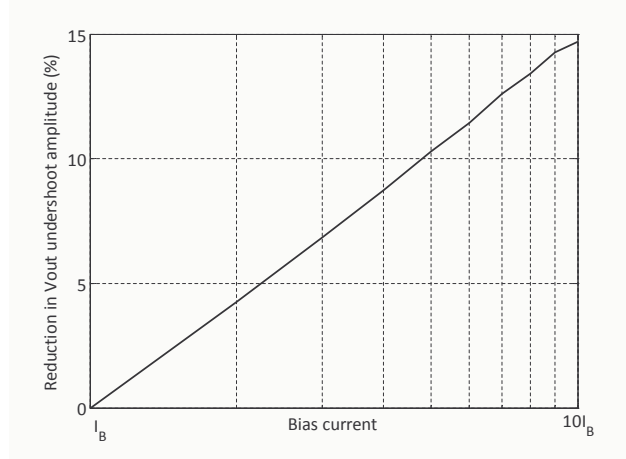


Figure 3.23: Reduction in output voltage undershoot amplitude versus bias current.

can be seen, the undershoot amplitude reduces as the bias current increases. In Section 4, several architectures that emphasize on improving the slew rate in CL-LDO voltage regulators will be discussed. The main idea behind all of them is increasing the charging/discharging current at the gate of the pass transistor during large load transient events.

3.5.3 Power Supply Rejection

3.5.3.1 PMOS Pass Transistor

Figures 3.24 and 3.25 show the PSR small-signal model for internally compensated LDOs with PMOS pass transistor with Type-A and Type-B EAs, respectively.

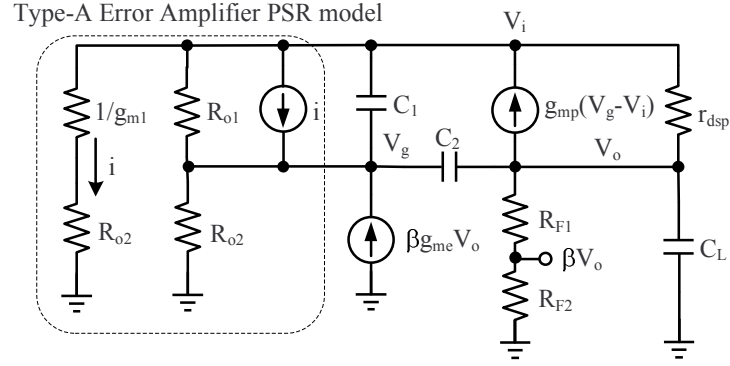


Figure 3.24: PSR small signal model for internally compensated LDO voltage regulator with PMOS pass transistor and Type-A EA.

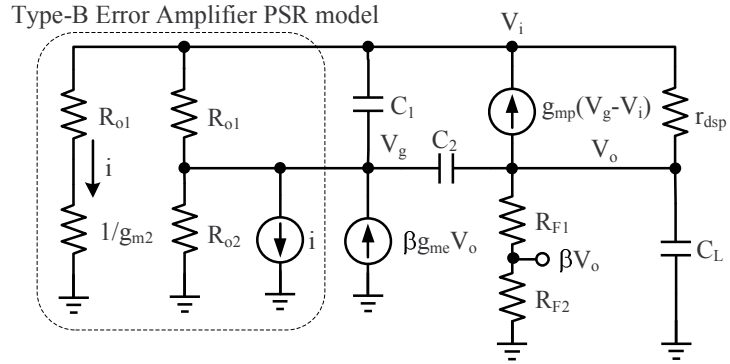


Figure 3.25: PSR small signal model for internally compensated LDO voltage regulator with PMOS pass transistor and Type-B EA.

These small-signal models are based on Figure 3.16(a).

The PSR transfer function can be approximated as,

$$\frac{V_o(s)}{V_i(s)} = PSR_{DC} \cdot \frac{(1 + \frac{s}{\omega_{z1,psr}}) \cdot (1 + \frac{s}{\omega_{z2,psr}})}{(1 + \frac{s}{\omega_{p1,psr}}) \cdot (1 + \frac{s}{\omega_{p2,psr}})} \quad (3.27)$$

where

$$PSR_{DC} \cong \frac{1 + g_{mp}r_{dsp}(1 - A_{PSR})}{\beta g_{mp}r_{dsp}g_{me}R_{oe}}, \quad \omega_{z2,psr} = \frac{g_{mp}}{C_1},$$

$$\omega_{p1,psr} = \frac{\beta g_{me}}{C_2}, \quad \omega_{p2,psr} = \frac{g_{mp}}{C_L \left(1 + \frac{C_1}{C_2}\right) + C_1}$$

Table 3.4 shows the analytical expressions for $\omega_{z1,psr}$ and $|PSR|_{DC}$ for an internally compensated LDO voltage regulator implemented with Type-A and Type-B error amplifiers. As can be seen from Table 3.4, the LDO voltage regulator implemented with a Type-A amplifier presents higher DC PSR than the one implemented with a Type-B amplifier for the same loop gain.

Table 3.4: Analytical expressions for PSR of an internally compensated LDO voltage regulator with PMOS Pass Transistor

Error Amplifier	A_{PSR}	$\omega_{Z1,psr}$	$ PSR _{DC}$
<i>Type – A</i>	1	$1/(g_{mp}r_{dsp}C_2R_{oe})$	$\frac{1}{\beta g_{me}R_{oe}g_{mp}r_{dsp}}$
<i>Type – B</i>	0	$1/(R_{oe}C_2)$	$\frac{1}{\beta g_{me}R_{oe}}$

3.5.3.2 NMOS Pass Transistor

Figures 3.26 and 3.27 show the PSR small signal model for internally compensated LDOs with NMOS pass transistor with Type-A and Type-B EAs, respectively. These small signal models are based on Figure 3.16(b). The PSR transfer function can be

approximated as,

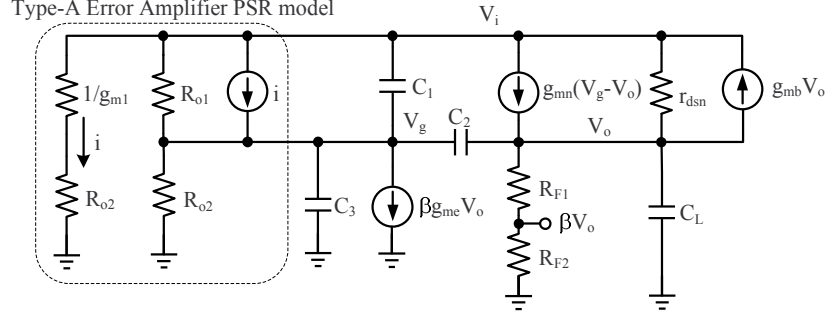


Figure 3.26: PSR small-signal model for externally compensated LDO voltage regulator with NMOS pass transistor and Type-A EA.

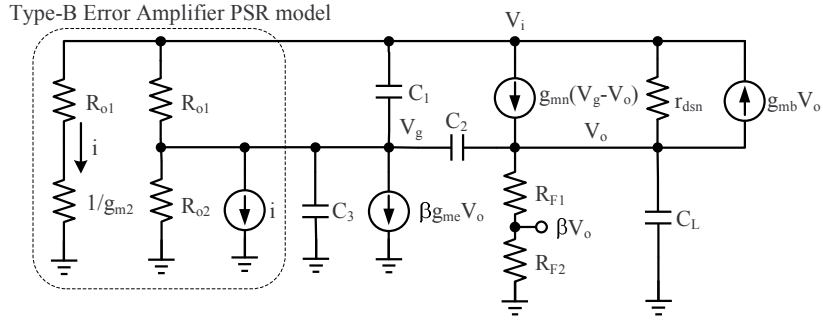


Figure 3.27: PSR small-signal model for internally compensated LDO voltage regulator with NMOS pass transistor and Type-B EA.

$$\frac{V_o(s)}{V_i(s)} = PSR_{DC} \cdot \frac{(1 + \frac{s}{\omega_{z1,psr}}) \cdot (1 + \frac{s}{\omega_{z2,psr}})}{(1 + \frac{s}{\omega_{p1,psr}}) \cdot (1 + \frac{s}{\omega_{p2,psr}})} \quad (3.28)$$

where

$$PSR_{DC} \cong \frac{1 + g_{mn} r_{dsp} A_{PSR}}{\beta g_{mn} r_{dsp} g_{me} R_{oe}}, \quad \omega_{z2,psr} = \frac{g_{mn}}{C_1},$$

$$\omega_{p1,psr} = \frac{\beta g_{me}}{C_2 + C_3}, \quad \omega_{p2,psr} = \frac{g_{mn}}{C_L \left(1 + \frac{C_1}{C_2 + C_3}\right) + C_1}$$

Table 3.5 shows the analytical expressions for $\omega_{z1,psr}$ and $|PSR|_{DC}$ for an internally compensated LDO voltage regulator implemented with NMOS pass transistor for Type-A and Type-B error amplifiers. As can be seen from Table 3.5, the LDO voltage regulator implemented with a Type-B amplifier presents higher DC PSR than the one implemented with a Type-A amplifier for the same loop gain.

Table 3.5: Analytical expressions for PSR of an internally compensated LDO voltage regulator with NMOS Pass Transistor

Error Amplifier	A_{PSR}	$\omega_{Z1,psr}$	$ PSR _{DC}$
<i>Type – A</i>	1	$1/(C_2 R_{oe})$	$\frac{1}{\beta g_{me} R_{oe}}$
<i>Type – B</i>	0	$1/(g_{mn} r_{dsn} R_{oe} C_2)$	$\frac{1}{\beta g_{me} R_{oe} g_{mn} r_{dsn}}$

3.5.4 PMOS Versus NMOS Pass Transistor

Table 3.6 compares CL-LDO voltage regulators implemented with NMOS and PMOS pass transistors. As can be observed in Table 3.6, CL-LDO voltage regulators implemented with PMOS pass transistors have smaller drop-out voltage than the ones implemented with NMOS. This make PMOS implementations more power efficient than NMOS implementations. Moreover, PMOS implementations operate with smaller input voltages than NMOS implementations for the same output voltage. The maximum current in NMOS implementations is smaller than PMOS implementations due to the limited voltage swing at the gate of the pass transistor. The drop-out voltage in a CL-LDO voltage regulator with NMOS pass transistor can be reduced if a charge pump is used to power the EA [19] or the pass transistor

is implemented with a natural V_{th} NMOS device.

Table 3.6: PMOS versus NMOS pass transistor comparison

Parameter	NMOS	PMOS
Drop-out voltage (V_{DO})	$V_{SD(sat)} + V_{th}$	$V_{SD(sat)}$
$V_{IN,min}$	$V_o + V_{DO}$	$V_o + V_{DO}$
Output Resistance	$\frac{1}{g_m}$	r_{ds}
$I_{o,max}$	Low	Moderate
Efficiency	Moderate	High
Transient Response	Fast	Moderate
PSR	Good	Moderate

NMOS implementations usually have better transient response than PMOS due to their small open loop output resistance. In addition, implementations with NMOS pass transistor offers better PSR performance for the same loop gain as shown in Figure 3.28. This is due to the fact that having the same loop gain implicates that $g_{me}R_{oe}$

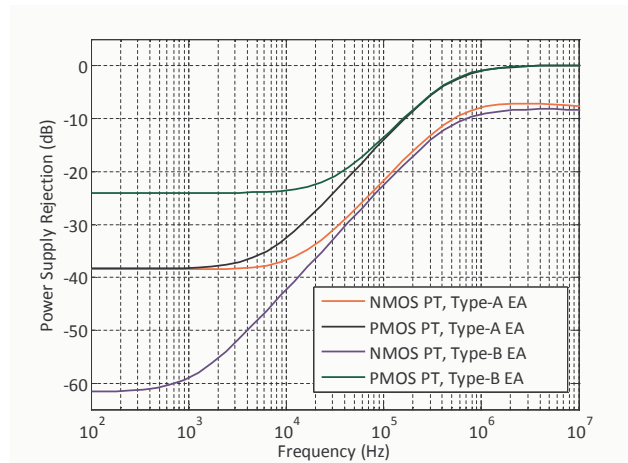


Figure 3.28: Internally compensated LDO voltage regulator PSR.

in (3.24) is greater than in (3.23) and hence, $\beta g_{mn} r_{dsn} g_{me} R_{oe} > \beta g_{mp} r_{dsp} g_{me} R_{oe}$. Moreover, the combination of the PMOS pass transistor with the load acts as a common gate amplifier from V_{IN} to V_{OUT} , while the combination of the NMOS pass transistor with the load acts as a voltage divider from V_{IN} to V_{OUT} ; as a result, the implementation with NMOS provides more isolation between the V_{IN} and V_{OUT} at high frequencies. This translates into better PSR performance at high frequencies for the implementation with a NMOS pass transistor.

3.6 Externally Versus Internally Compensated LDO Voltage Regulators

Table 3.7 qualitatively compares externally and internally compensated LDO voltage regulators [7]. As can be seen, externally compensated LDO voltage regula-

Table 3.7: Externally versus internally compensated LDO voltage regulators comparison

	Externally Compensated	Internally Compensated
Application	Higher Power (E.g. heavier loads)	Lower Power (E.g. lighter loads)
Load Capacitor C_L	Off-chip or in-package	On-chip or in-package
Load Transient	Better (E.g. smaller $\Delta V_{OUT} \propto 1/C_L$)	Worse (E.g. larger ΔV_{OUT})
Worst Case Stability	Large I_L	Small I_L
PSR	Better (E.g. higher ω_{p1})	Worse (E.g. lower ω_{p1})
Cost	Higher	Lower

tors exhibit in general better performance than internally compensated ones at the expense of higher cost. The off-chip capacitor C_L provides low output impedance in externally compensated LDO voltage regulators. This reduces the voltage dips/surges

during load transient events when compared with internally compensated LDO voltage regulators. For the same reason, externally compensated LDO voltage regulators can deal with heavier loads than internally compensated ones.

3.7 Guidelines for Measuring LDO Voltage Regulators

LDO voltage regulator measurements include: efficiency, load regulation/transient, line regulation/transient, and PSR. Basic voltage regulator characterization requires the following measurement equipment: power supplies, multi-meters, an oscilloscope, waveform generators, power resistors, and an evaluation board.

3.7.1 Efficiency Measurement Setup

The power efficiency of a voltage regulator is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L V_{OUT}}{I_{IN} V_{IN}} \leq \frac{I_L V_{OUT}}{I_{IN} (V_{OUT} + V_{DO})} \quad (3.29)$$

where I_L represents the load current and V_{OUT} represents the output voltage. Parameters V_{IN} and I_{IN} represent the input voltage and current of the LDO voltage regulator, respectively. Hence, efficiency can be calculated by measuring I_L , V_{OUT} , I_{IN} , and V_{IN} with a multi-meter.

3.7.2 Load Transient Measurement Setup

Figure 3.29 shows a load transient measurement setup. The load step is generated by switching the connection between the output voltage V_{OUT} and the load resistance R_L using the power FET M_{TEST} . The minimum load current ($I_{L,min}$) is determined by V_{OUT}/R_{LB} and the maximum load current is equivalent to $I_{L,min} + V_s/R_L$. The output voltage and load current step waveforms can be observed in an oscilloscope since I_L is directly proportional to R_L . Load regulation can be obtained if the measurements are performed in steady state.

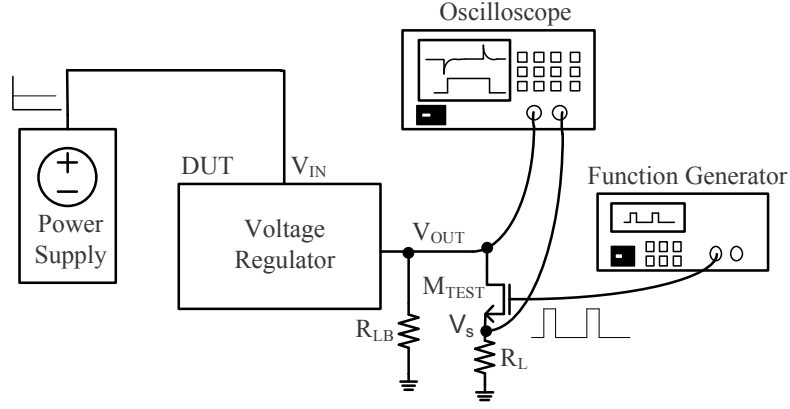


Figure 3.29: Load transient measurement setup.

3.7.3 Line Transient Measurement Setup

Figure 3.30 shows a line transient measurement setup. The line transient test can be performed with a square signal superimposed on a DC voltage level. A driver is added between the waveform generator and the input of the voltage regulator to provide the required input current. This is particularly necessary at heavy loads since a waveform generator is not capable of providing currents above a few milliamps. In addition, this driver needs to be able to handle the input capacitance of the LDO voltage regulator. Line regulation can also be obtained if the measurements are performed in steady state.

3.7.4 PSR Measurement Setup

The measurement setup for line transient (Figure 3.30) can be used for PSR. The only difference is that a sinusoidal signal instead of a square signal is imposed on a DC voltage level. The peak-to-peak amplitude of the sinusoidal signal is typically in the order of 20-100 mV [7]. The PSR is the ratio between V_{OUT} and V_{IN} and can be obtained using an oscilloscope. Due to the amplitude of the sinusoidal signal, PSR

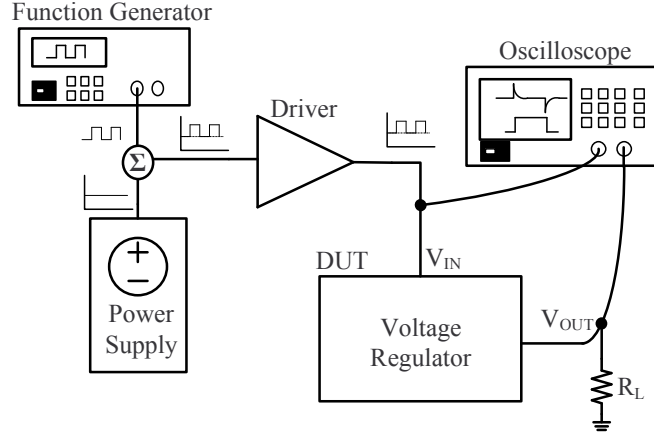


Figure 3.30: Line transient measurement setup.

simulation results based on AC analysis may not correlate with measurement results. Hence, PSR simulation results based on transient simulations may correlated better with experimental results since the test bench is closer to the actual one used in measurements [7].

3.8 Design Strategy in LDO voltage regulators

Figure 3.31 shows a design flow for LDO voltage regulators. It begins with the basic DC requirements V_{IN} , V_{OUT} , I_L , and I_Q specifications. From these specifications, the dimensions of the pass transistor can be chosen:

$$\frac{W}{L} = \frac{2I_L}{K_p (V_{DS,sat})^2} = \frac{2I_L}{K_p (V_{DO})^2} \quad (3.30)$$

Minimum length is typically chosen to minimize the gate capacitance of the pass transistor which affects the stability, transient response, and PSR performance. The feedback resistors can be chosen from the ratio between the V_{OUT} and V_{REF} and I_Q specifications:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{F1}}{R_{F2}}\right) \quad (3.31)$$

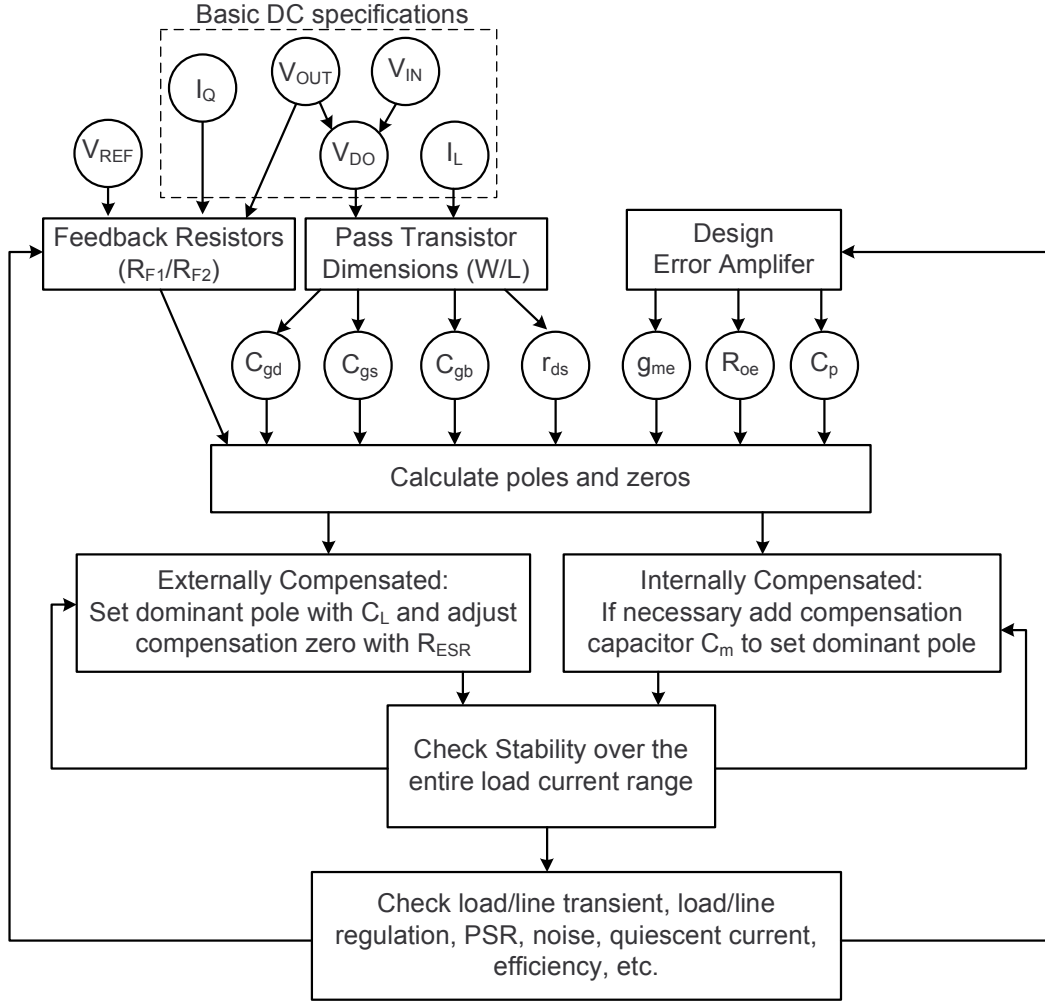


Figure 3.31: Low dropout voltage regulator design flow.

$$H \cdot I_Q = \frac{V_{OUT}}{R_{F1} + R_{F2}} \quad (3.32)$$

where $H \cdot I_Q$ is a percentage of the total quiescent current budget. The feedback resistors can be found using (3.31) and (3.32). The poles and zeros can be estimated from the pass transistor dimensions, feedback resistors, and error amplifier small signal parameters. Then, on an externally compensated LDO, the C_L capacitor can be chosen to set the dominant pole and R_{ESR} to place the compensation zero at

the desired location for stability purposes. In the case of an internally compensated LDO, a compensation capacitor can be used to set the dominant pole. The loop's stability can be verified by following the proposed procedure. After verifying stability, performance parameters (e.g., load/line regulation, PSR) can be simulated to check if specifications are met. Otherwise, the pass transistor dimensions, feedback resistors values and/or EA design (e.g., bias current, compensation capacitance, transistor dimensions, etc.) can be modified.

In summary, the LDO voltage regulator design starts with the pass transistor or feedback resistors, and then EA. Next, specifications are verified, and if necessary, the pass transistor, feedback resistors, and EA can be modified to meet requirements.

3.9 Practical Design Considerations for LDO Voltage Regulators

3.9.1 Pass Transistor

3.9.1.1 Design

As explained previously in this section, the pass transistor design affects the efficiency, PSR, transient, minimum input voltage, and maximum delivered load current (see Table 3.6). The noise contribution of the pass transistor is typically neglectable when compared with the first stage of the EA and feedback resistors contribution. Moreover, the dimensions of the pass transistor can be calculated based on V_{IN} , V_{OUT} , and I_L as shown in (3.30). For a PMOS pass transistor assuming operation in the saturation region, the dimensions can be calculated using the following equation:

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{2I_{L,max}}{K_p(V_{DS,sat})^2} = \frac{2I_{L,max}}{K_p(V_{DO})^2} \quad (3.33)$$

and for an NMOS pass transistor, the dimensions can be obtained with:

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{2I_{L,max}}{K_n (V_{DS,sat})^2} = \frac{2I_{L,max}}{K_n (V_{DO})^2} \quad (3.34)$$

Notice that in (3.34), it is assumed that voltage at the gate of the pass transistor could go above V_{IN} to provide the necessary maximum load current. This can be achieved using a charge pump to bias the error amplifier. For the same $V_{DS,sat}$, the dimensions of the pass transistor implemented with NMOS and PMOS are related by:

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{K_n}{K_p} \left(\frac{W}{L}\right)_{NMOS} \quad (3.35)$$

Typically, $K_n \geq 3K_p$ and as a result, a P-Type pass transistor generally occupies a larger area than the N-Type. However, for a fair comparison the area occupied by the charge pump (e.g., capacitors) needs to be included.

Due to the large I_L range in most LDO voltage regulators, the pass transistor may operate over three different regions (e.g., subthreshold, saturation, triode regions). This complicates the modeling of the pass transistor since an I_L dependent model is required to represent the pass transistor's parameters (e.g., g_m , g_{ds} , c_{gs}) over the entire I_L range (see Figures 3.21 and 3.22 for details). Therefore, two possibilities to model the pass transistor are: a) using a piece-wise approximation where the switching points are defined by the operating region and each parameter is defined according to its respective equation for each operating region or b) using a general polynomial expression as:

$$P(I_L) = p_0 + p_1 I_L + p_2 I_L^2 + \dots + p_n I_L^n \quad (3.36)$$

where p_i (for $i = 0, 1, 2, \dots, n$) are the coefficients for a fitted polynomial for each

parameter in terms of I_L .

3.9.1.2 Layout

The track resistance (resistance between drain/source and bondpad), bond-wire resistance (resistance between bondpad and pin), and printed board circuit trace resistance affect the effective drop-out voltage [7]. To minimize the track resistance, use as many contacts and wide tracks for the drain and source terminals to minimize sheet and via resistances. This is critical since these terminals carry the load current. Also, the pass transistor should be placed as close as possible to the bondpad to minimize track resistance [7]. Top metals should be used for power routing since they have the smallest resistance. In addition, multiple metals in parallel can be used to minimize the track resistance. To reduce the bond-wire resistance and inductance, multiple parallel bond-wires can be used for the drain and source terminals. To minimize the effect of the bond-wire resistance in the load regulation, the output voltage is sensed at the pin instead of the drain/source of the PMOS/NMOS pass transistor. By doing this, the bond-wire resistance is included in the feedback loop and as a result, better load regulation is achieved. This technique requires an additional bondpad and bond-wire. The output of the pass transistor is connected to V_{OUT} pin through V'_{OUT} bondpad and a bondwire; and the feedback resistors are connected to V_{OUT} pin through V_{SENSE} bondpad and another bondwire as shown in Figure 3.4. This technique is known as the *Kelvin* or *Star* connection [7].

3.9.2 Error Amplifier

3.9.2.1 Design

The accuracy and quiescent power consumption of the LDO voltage regulator are highly dependent on the EA design. As already explained in this section, line/load regulation and DC PSR are inversely proportional to the DC gain of the EA. More-

over, the DC PSR also depends on the Type of EA (e.g., Type-A or Type-B). The EA's bandwidth affects the load/line transient performance of the LDO voltage regulator. Typically, a multi-stage EA is implemented to deal with the gain and bandwidth challenges. The first stage usually provides most of the DC gain and the last stage typically consumes most of the quiescent current to place the non-dominant pole beyond UGF and improve the slew rate at the gate of the pass transistor. The differential pair of the EA should be sized carefully to minimize the flicker noise without increasing too much the input capacitance of the EA. If the input capacitance is large enough, it can generate an undesirable pole that affects the loop's stability. In battery-powered applications, the EA must be designed to meet all the specifications with the smallest amount of quiescent current to extend the battery life. The systematic and random offsets of the EA should be minimized since it can affect the regulation of the system. In addition, the EA should be able to operate properly for the input voltage range, voltage reference voltage, and load current range which modifies the output voltage swing of the EA. Hence, an EA with high DC gain, high bandwidth, low I_Q , low noise, and low input offset is desired [7].

3.9.2.2 Layout

The error amplifier should be laid out using standard layout techniques such as common centroid and interdigitized configurations and use dummy components for best matching [20]. The differential pair and active current load require critical matching to minimize offset as well as placing as many substrate contacts as possible in local cells to provide homogeneous bulk voltage for the transistors. This minimizes threshold voltage variation among them. Using P+ guard ring and N+ guard ring for NMOS and PMOS transistors, respectively [21]. Figure 3.32 shows an example of an error amplifier transistor level implementation and layout with the suggestions

previously mentioned.

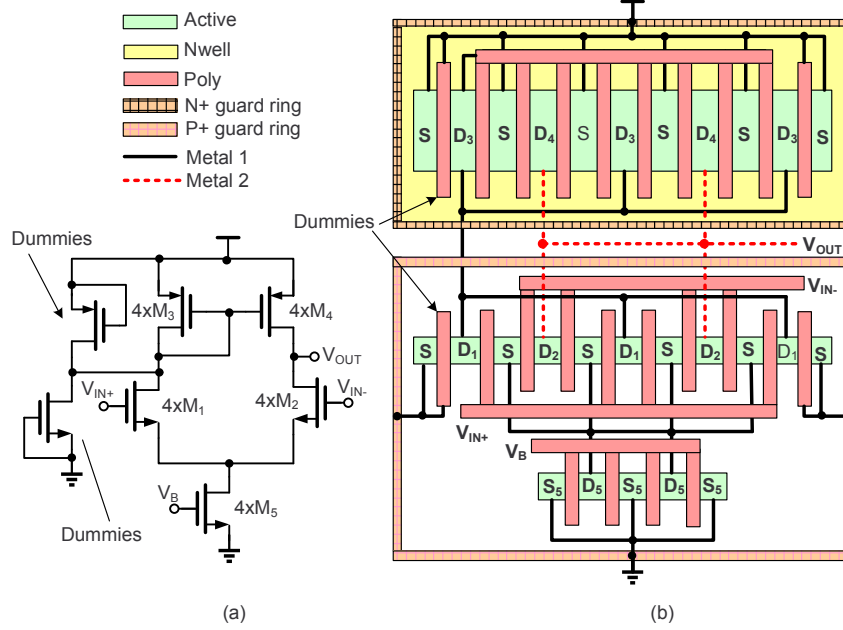


Figure 3.32: Example of an error amplifier (a) transistor level (b) layout implementation.

3.9.3 Printed Board Circuit

3.9.3.1 Design

Using ceramic capacitors with low ESR at the output to minimize voltage dip/surge amplitudes ($I_L R_{ESR}$) during load transient events. Multiple capacitors can be used in parallel to increase the capacitance and reduce R_{ESR} to improve even further the load transient response. It is advised to place a capacitor from the input of the LDO voltage regulator to ground to reduce the input voltage ripple and spikes before they reach the LDO voltage regulator [22]. In addition, it is also advised to include the capacitor model in simulations. Figure 3.33 shows a model for an off-chip capacitor

that includes the effect of the R_{ESR} and equivalent series inductance (ESL). Ideally, a capacitor behaves as a short circuit at high frequencies, but due to the R_{ESR} and ESL it behaves as an open circuit. In this case, the output capacitor in an externally compensated LDO voltage regulator behaves as a high impedance, and as a result, PSR may be degraded because the output voltage ripple could be amplified at high frequencies [10].



Figure 3.33: Off-chip capacitor model that includes R_{ESR} and ESL .

3.9.3.2 Layout

Using short and wide traces for power routing lines (E.g. V_{IN} and V_{out}) to minimize trace resistance and as a result, reduce power losses.

4. LOW DROP-OUT VOLTAGE REGULATORS: CAPACITOR-LESS ARCHITECTURE COMPARISON*

4.1 Introduction

Demand for system-on-chip solutions has increased the interest in LDO voltage regulators which do not require a bulky off-chip capacitor to achieve stability, also called capacitor-less LDO (CL-LDO). Several architectures have been proposed; however comparing these reported architectures proves difficult, as each has a distinct process technology and specifications. This chapter compares CL-LDOs in a unified matter. We designed, fabricated, and measured five illustrative CL-LDO regulator topologies [18], [23]-[26] in the same process (0.5 μ m CMOS) under common design specifications to facilitate comparison. We compare the architectures in terms of (1) line/load regulation, (2) power supply rejection, (3) line/load transient, (4) total on-chip compensation capacitance, (5) noise, and (6) quiescent power consumption. Our remarks and observations are suitable for the chosen design constraints.

This chapter presents representative CL-LDO regulator topologies [18], [23]-[26] and [27]-[44]. In addition, remarks on CL-LDO regulator architectures and experimental results are provided. Finally, conclusions are drawn.

4.2 Comparison of CL-LDO Regulator Topologies

We categorize several illustrative CL-LDO regulator topologies into 3 groups. In this section, it is assumed that the gain stages are powered from V_{IN} unless otherwise specified.

*This section is reprinted with permission from “Low Drop-Out Voltage Regulators: Capacitor-Less Architecture Comparison” by J. Torres et al., accepted for future publication in *IEEE Circuits and Systems Magazine*.

4.2.1 Advanced Compensation Topologies

Topologies [18] and [23] are two of the first CL-LDO regulators. They are based on Miller pole splitting compensation to achieve small on-chip compensation capacitance when compared with the conventional (externally compensated) LDO regulator. In Figure 4.1 (a) [18], a damping-factor circuit stabilizes the LDO regulator for various capacitive load conditions. The LDO regulator requires the damping factor compensation (DFC) circuit to be stable with and without an off-chip capacitor. In a capacitor-less configuration, the damping factor circuitry might not be necessary since the feedback loop is effectively compensated with the Miller-compensation capacitor C_m . The dominant pole is given by $A_2 A_p C_m$ and the output resistance of the EA first stage A_1 . A_p is the gain of the pass transistor. In this chapter, we will refer to this topology as the Damping Factor architecture. Figure 4.1(b) shows

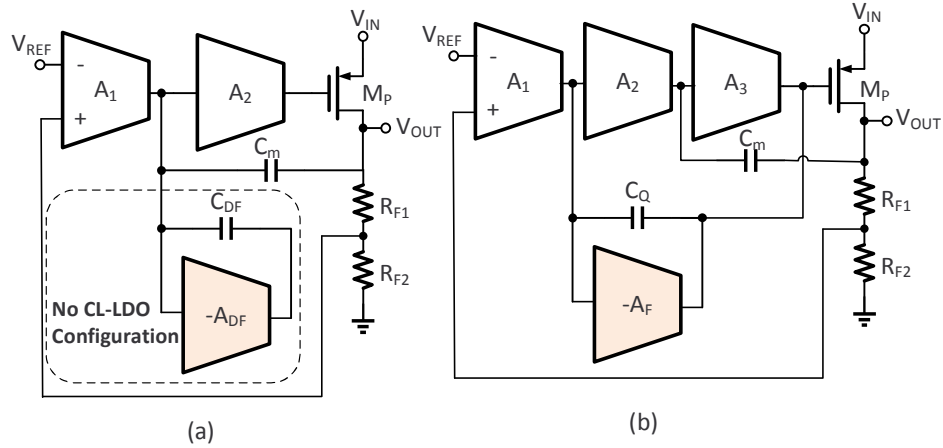


Figure 4.1: CL-LDOs with improved frequency compensation techniques (a) DFC [18], (b) Q-Reduction [23].

the Q-reduction architecture. This architecture was proposed to minimize on-chip

capacitance and quiescent current [23]. The Q-reduction circuit is formed by C_Q and the transconductance A_2 . The Q-reduction technique controls the Q of the non-dominant complex poles to improve the stability at light loads.

4.2.2 Load Transient Topologies

Approaches that improve the load transient comprise either pass-transistor-gate-voltage slew-rate enhancement with multiple active loops [25]-[34] and/or output-impedance reduction [35]-[39].

Architecture in [26] and [27] employ a current amplifier A_i in series with capacitance C_f that acts as an auxiliary fast loop in addition to the main voltage loop as shown in Figure 4.2 (a). The capacitance C_f reacts to sudden changes on V_{OUT} during load transients by generating an equivalent transient current (i_f). Then, current i_f is amplified by the gain A_i and injected into the pass transistor's gate capacitance. Thus, this auxiliary loop improves the transient response. Moreover, it helps to achieve internal compensation since the dominant pole of the system is defined by $\omega_d \cong 1/(A_i A_p C_f R_{oi} || R_{o1})$ where R_{oi} and R_{o1} are the output resistances of A_i and A_1 , respectively. [28] expands on this technique, employing a bi-directional, asymmetric current amplifier to increase the UGF by cancelling the RHP zero from the pass-transistor C_{gd} . Figure 4.2(b) displays a CL-LDO with multiple loops to improve the settling response [25]. This CL-LDO regulator combines a current-sensing transistor M_s and a transimpedance amplifier A_{TRANS} to generate an additional fast loop. Load variations are detected by M_s to generate a scaled copy of I_L . During transitions from low to high load currents, the corresponding increase in the sense current improves the slew rate at the gate of the pass transistor. In Figure 4.2(c) [29], an EA with push-pull output stage achieves high slew rate at the gate of the pass transistor and reduces the quiescent current consumption. Class AB operation improves the

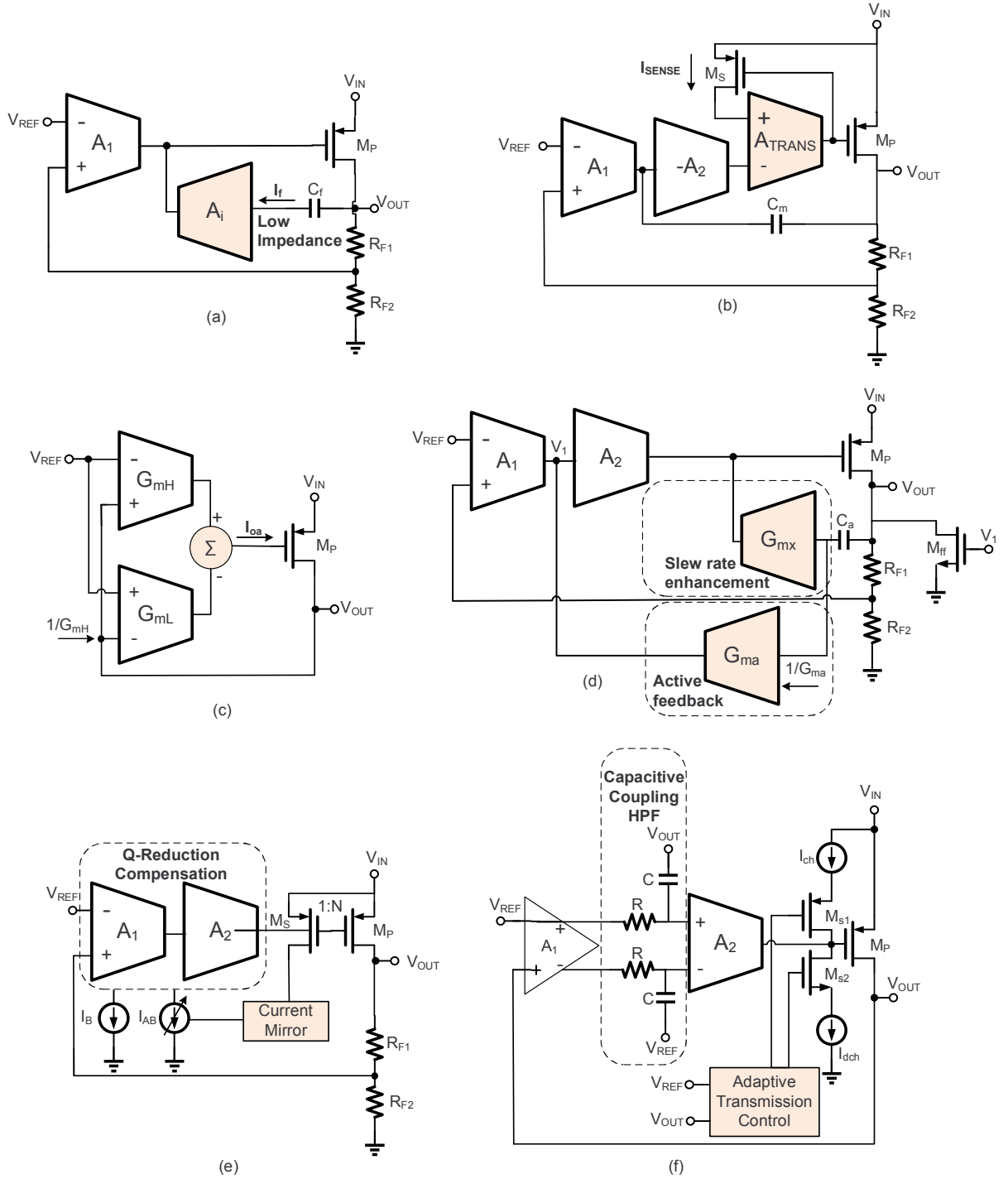


Figure 4.2: CL-LDOs with multi-feedback loops (a) Differentiator [26], (b) Transimpedance [25], (c) High Slew Rate EA [29], (d) AFC&SRE [30], (e) Adaptively Biased [32], and (f) Capacitive Coupling & ATC [33].

slew rate since during transient events the peak currents of transconductors G_{mH} and G_{mL} are not limited by the bias current.

The CL-LDO regulator in Figure 4.2(d) [30] combines active feedback compensation (AFC) G_{ma} and slew-rate-enhancement (SRE) G_{mx} techniques to increase the loop bandwidth, reduce the total on-chip capacitance compensation, and improve the slew rate at the gate of the pass transistor. The slew-rate enhancement block reduces V_{OUT} variations during load current transients events. The combination of M_{ff} with M_P creates a weak push-pull at V_{OUT} to reduce the overshoots during load transients. A similar architecture is presented in [31].

In Figure 4.2(e) [32], a CL-LDO regulator uses an auxiliary loop to adjust the bias current of the EA's first stage. The EA is biased with a small fixed I_B and an adaptive bias current I_{AB} proportional to I_L . The auxiliary loop is formed by the current sensing transistor M_s and a simple current mirror. The adaptive bias current I_{AB} increases the loop bandwidth and, as a result, the load transient performance is improved.

A multi-loop CL-LDO regulator that improves load/dynamic voltage scaling transient response is shown in Figure 4.2(f) [33]. The first loop employs a capacitively coupled high-pass filter that detects voltage variations at V_{REF} and V_{OUT} to increase the slew rate at the gate of the pass transistor. This increase in the slew rate improves the transient response. The second loop comprises the adaptive transmission control (ATC) block, two switches M_{s1} and M_{s2} , and the current sources I_{ch} and I_{dch} . This loop detects large voltage variations of V_{OUT} and V_{REF} , compares them with reference voltages V_H/V_L (not shown), and decides whether to enable M_{s1} or M_{s2} to charge or discharge the pass-transistor gate. A multi-loop CL-LDO structure for SRAM bank designed for very fast load step response while maintaining low quiescent current is presented in [34].

Multiple CL-LDO regulator topologies with a power stage based on the flipped voltage follower (FVF) have been proposed [35]-[39]. These kind of topologies were not fabricated in this work, but are included in the discussion for the sake of completeness. The FVF exhibits low output impedance due to shunt feedback, thus yielding good load regulation and stability [36]. The basic FVF CL-LDO regulator consists of pass transistor M_P , control transistor M_c , and current source I_B as shown in Fig. 4.3. Voltage V_{CTRL} sets $V_{OUT} = V_{SG,MC} + V_{CTRL}$. Transistor M_c source ter-

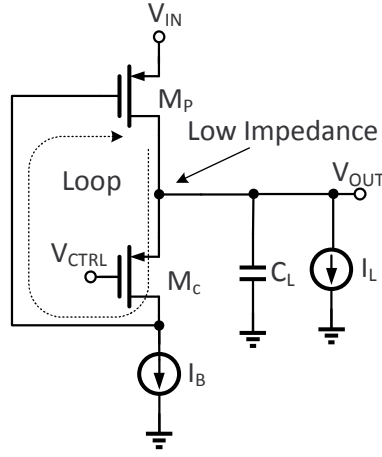


Figure 4.3: CL-LDOs based on FVF [35]-[39].

minal senses variations at V_{OUT} and then amplifies the error signal to control the gate voltage of M_P . This mechanism regulates V_{OUT} and generates the required current by the load. Several architectures [37]-[39] have been proposed to improve the slew rate at the gate of M_P and increase the loop gain.

4.2.3 PSR Topologies

Fig. 4.4 shows several topologies that have been proposed to improve PSR [24], [40]-[44]. The compensation schemes are not included to simplify the diagrams.

In Figure 4.4(a) [40], a NMOS in cascode with the PMOS pass transistor is added to

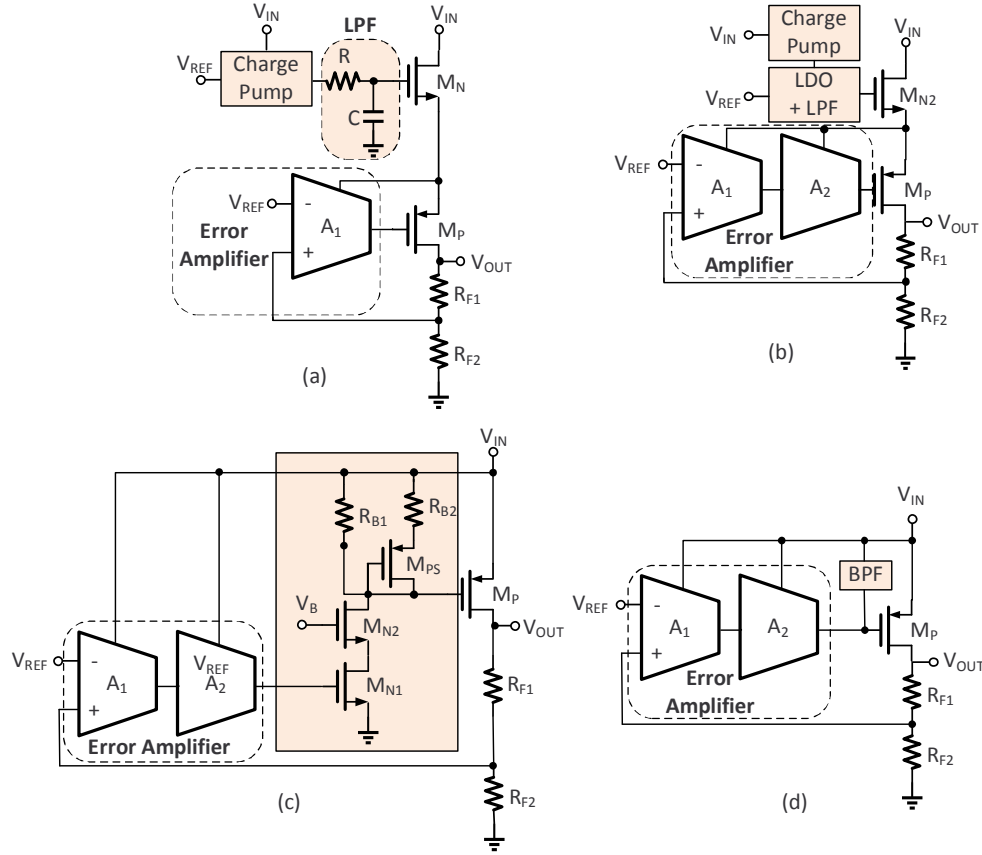


Figure 4.4: CL-LDOs for PSR enhancement (a) NMOS Cascode [40], (b) NMOS Cascode with auxiliary LDO [41, 42], (c) Voltage Subtractor [24], (d) FF with BPF [44].

increase the isolation between V_{IN} and V_{OUT} . A charge pump generates a large voltage at the gate of the NMOS transistor to reduce its drop out voltage. In addition, a first-order low pass filter (LPF) is placed between the output of the charge pump and the gate of the NMOS device to reduce the charge pump output ripple. In Figure 4.4(b) [41], [42] an NMOS cascoded with the PMOS transistor is used as well, but the gate bias of the NMOS is controlled with an LDO regulator and first order

LPF. This implementation can potentially reduce the area when compared with [40] since the amplifier consumes low current from the charge pump which reduces the size of its capacitors. In addition, it relaxes the cut-off frequency of the LPF due to smaller ripple at the output of the charge pump, thus potentially saving area. All these works provided very good PSR but they increase the drop-out voltage of the LDO. In Figure 4.4(c) [24] and [43], the main idea to provide high impedance from the gate of M_P to ground and a low impedance from the gate of M_P to V_{IN} .

This allows the gate to follow the signal at the source of M_P such that the EA behaves like a Type-A amplifier ($A_{psr} \cong 1$); and as a result, PSR at low frequencies is improved. In Figure 4.4(c) [24], R_{B1} , R_{B2} , and M_{PS} form the low impedance from the gate of M_P to V_{IN} , and M_{N2} & M_{N1} form the high impedance from the gate to ground. A topology with a power-supply-rejection boosting filter circuit is shown in Figure 4.4(d) [44]. This topology adds a feedforward (FF) path with bandpass transfer function to improve the power supply rejection at middle-to-high frequency over a wide loading range.

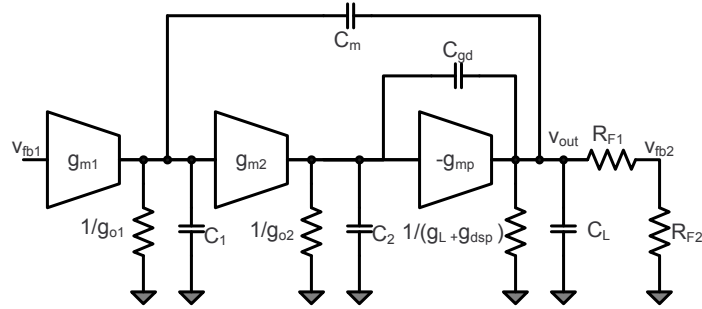


Figure 4.5: CL-LDO regulator with damping factor technique small-signal model.

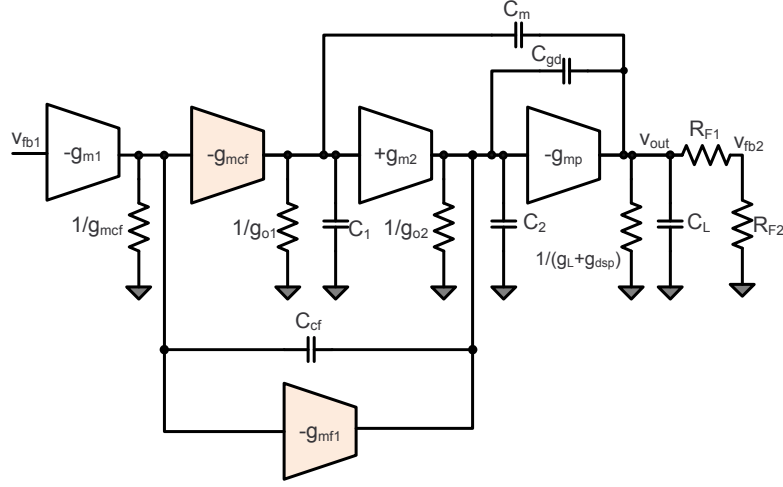


Figure 4.6: CL-LDO regulator with Q-reduction technique small-signal model.

4.3 Selected Topologies

For comparison, we select at least one representative architecture from each of the three groups (Advanced Compensation, Load Transient, and PSR). The selected the following architectures: [18], [23]-[26] (Figure 4.1(a), Figure 4.1(b), Figure 4.4(c), Figure 4.2(b), and Figure 4.2(a)).

The small-signal models for the Damping Factor, Q-Reduction, Voltage Subtractor, Transimpedance, and Differentiator CL-LDO regulators are shown in Figure 4.5, Figure 4.6, Figure 4.7, Figure 4.8, and Figure 4.9, respectively. Parameters g_{mi} , g_{oi} , and C_i (for $i = 1, 2$) represent the transconductances, the output conductances, and the parasitic capacitors of each stage, respectively. C_{gd} and g_{mp} are the gate to drain capacitance and transconductance of the pass transistor. C_L and g_L are the load capacitance and conductance, respectively. C_m represents a compensation capacitor. In Figure 4.5, notice that the damping factor circuit is not included because as mentioned in [18] it has no effect for capacitor-less operation and small load currents. In Figure 4.6, the Q-reduction circuit is formed by C_{cf} and a current

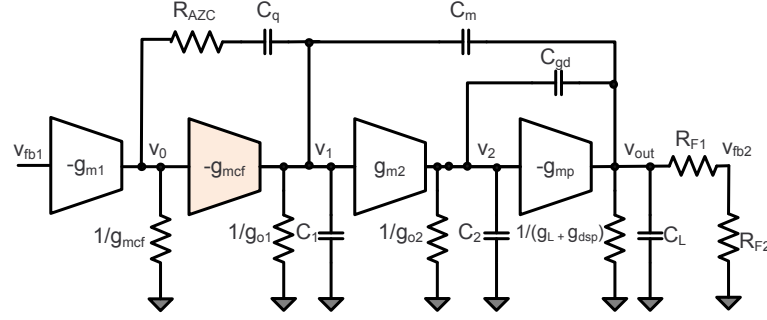


Figure 4.7: CL-LDO regulator with voltage subtractor technique small-signal model.

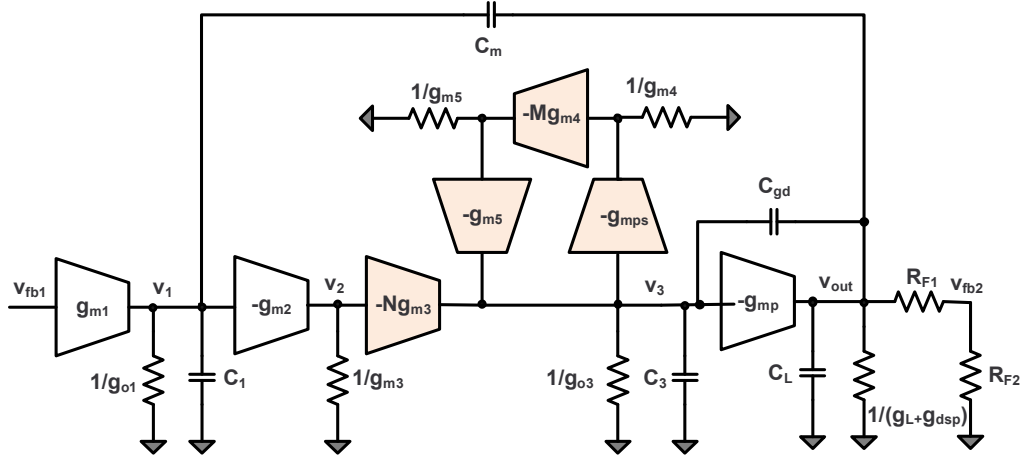


Figure 4.8: CL-LDO regulator with transimpedance technique small-signal model.

buffer of transconductance g_{mcf} . Also, a feed-forward transconductance stage (g_{mf1}) generates a left-half-plane (LHP) zero to improve the stability. In Figure 4.7, C_q and R_{AZC} generate a pole-zero pair to improve the stability of the CL-LDO regulator. In Figure 4.8, the transimpedance circuit is composed of transconductances g_{m3} , g_{m4} , and g_{m5} . g_{mps} and g_{mp} are the transconductance of the current sensing transistor and pass transistor, respectively. In the original implementation, the minimum load current was 10 mA. In this dissertation, the compensation capacitor C_m was con-

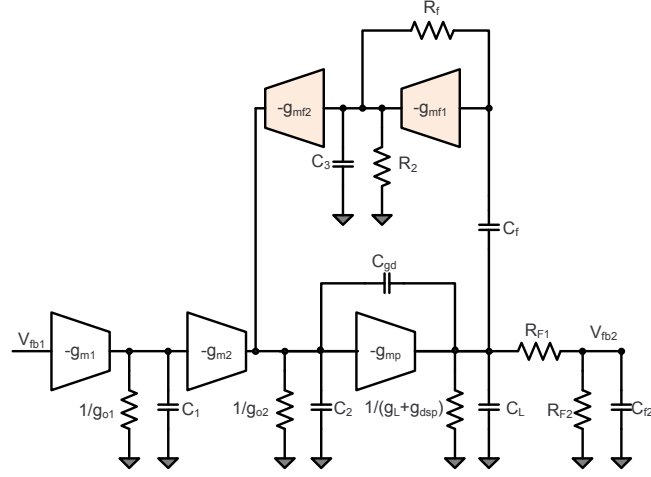


Figure 4.9: CL-LDO regulator with differentiator technique small-signal model.

nected at V_1 instead of V_2 to achieve stability at a minimum load current of $100\mu\text{A}$. In Figure 4.9, g_{mf1} and g_{mf2} , C_f , and R_f form the differentiator circuit. C_{f2} generates a high-frequency pole for stability purposes.

The loop transfer functions for the chosen topologies can be expressed as,

$$\frac{V_{fb2}(s)}{V_{fb1}(s)} \cong \frac{\beta \cdot A_{EA,o} \cdot \left(\frac{g_{mp}}{g_{out}}\right) \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p4}}\right) \cdot \left(\frac{s^2}{\omega_o^2} + \frac{s}{\omega_o Q} + 1\right)} \quad (4.1)$$

Tables 4.1 and 4.2 show approximated expressions for $A_{EA,o}$, ω_{p1} , ω_o , Q , ω_{z1} , and ω_{p4} for each CL-LDO regulator topology. In Table 4.1, $A_{dif} = g_{mf1}g_{mf2}R_fR_2$.

The PSR transfer function for all the topologies can be expressed as,

$$\frac{V_{out}(s)}{V_{in}(s)} \cong PSR_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{z1,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{z2,psr}}\right)}{\left(1 + \frac{s}{\omega_{p1,psr}}\right) \cdot \left(1 + \frac{s}{\omega_{p2,psr}}\right)}, \quad (4.2)$$

where

$$PSR_{DC} = \frac{1 + g_{mp}r_{dsp}(1 - A_{PSR})}{\beta g_{mp}r_{dsp}A_{EA,o}}.$$

Table 4.1: CL-LDO regulator loop small signal parameters ($A_{EA,o}$, ω_{p1} , ω_o)

Topologies	$A_{EA,o}$	ω_{p1}	ω_o
Damping Factor [18]	$\frac{g_{m1}g_{m2}}{g_{o1}g_{o2}}$	$\frac{g_{o1}g_{o2}g_{out}}{C_m g_{m2}g_{mp}}$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2(C_{gd}+C_L)}}$
Q-Reduction [23]	$\frac{g_{m1}}{g_{o1}} \left(\frac{g_{m2}}{g_{o2}} + \frac{g_{mf1}g_{o1}}{g_{mcf}g_{o2}} \right)$	$\frac{g_{o1}g_{o2}g_{out}}{C_m g_{m2}g_{mp}}$	$\sqrt{\frac{g_{m2}g_{mp}}{(C_{gd}+C_2+C_{cf})C_L}}$
Voltage Subtractor [24]	$\frac{g_{m1}g_{m2}}{g_{o1}g_{o2}}$	$\frac{g_{o1}g_{o2}g_{out}}{C_m g_{m2}g_{mp}}$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2 C_L}}$
Transimpedance [25]	$\frac{g_{m1}N g_{m2}}{g_{o1}g_{o3}(1+M\frac{g_{mps}}{g_{o3}})}$	$\frac{g_{o1}g_{o3}g_{out}(1+M\frac{g_{mps}}{g_{o3}})}{(N g_{m2}g_{mp}+M g_{mps}g_{out})C_m}$	$\sqrt{\frac{N g_{m2}g_{mp}}{C_{gd}(C_L+C_2)}}$
Differentiator [26]	$\frac{g_{m1}g_{m2}}{g_{o1}g_{o2}}$	$\frac{g_{o2}}{A_{dif} \frac{g_{mp}}{g_{out}} C_f + \left(1 + \frac{g_{mp}}{g_{out}}\right) C_{gd} + C_2}$	$\sqrt{\frac{g_{o1}}{C_1 C_{f2}(R_{F1} R_{F2})}}$

 Table 4.2: CL-LDO regulator loop small signal parameters (Q , ω_{z1} , ω_{p4})

Topologies	Q	ω_{z1}	ω_{p4}
Damping Factor [18]	$\frac{g_{m2}g_{mp}}{\omega_o(g_{mp}-g_{m2})C_{gd}}$	-	-
Q-Reduction [23]	$\frac{g_{m2}/\omega_o}{C_{gd}\left(1-\frac{g_{m2}}{g_{mp}}\right) + \frac{C_{cf}C_3g_{m2}}{C_m g_{mp}} + \frac{C_{cf}g_{m2}}{g_{mcf}}}$	$\frac{g_{m1}g_{m2}}{C_m g_{mf1}}$	-
Voltage Subtractor [24]	$\frac{g_{m2}g_{mp}/\omega_o}{(g_{mp}-g_{m2})C_{gd} + \frac{(1+2C_q/C_m)C_2C_L}{(1/g_{mcf}+R_{AZC})C_q}}$	$\frac{1}{R_{AZC}C_q}$	$\frac{g_{mcf}}{C_q}$
Transimpedance [25]	$\frac{N g_{m2}g_{mp}}{\omega_o((g_{mp}-N g_{m2})C_{gd})}$	-	-
Differentiator [26]	$\frac{1}{\omega_o\left(\frac{C_1}{g_{o1}} + C_{f2}(R_{F1} R_{F2})\right)}$	-	-

Table 4.3 shows approximate analytical expressions for $\omega_{z1,psr}$, $\omega_{z2,psr}$, $\omega_{p1,psr}$, $\omega_{p2,psr}$, and A_{PSR} for each CL-LDO regulator topology. Note that these EA topologies are more complex than the ones discussed in chapter 3 and as a result $-0.2 \leq A_{PSR} \leq 1.43$.

The voltage subtractor and damping factor topologies have good high frequency PSR since their $\omega_{z1,psr}$ is located at higher frequencies. The voltage subtractor has very good low-frequency PSR at light loads because its A_{PSR} is approximately 1 and high DC loop gain. The Q-reduction architecture also has excellent low-frequency PSR because of its high DC loop gain. However, its PSR bandwidth is limited due

Table 4.3: CL-LDO regulators PSR analytical expressions

Topologies	Damping Factor [18]	Q-Reduction [23]	Voltage Subtractor [24]	Transimpedance [25]	Differentiator [26]
$\omega_{z1,psr}$	$\frac{1-A_{psr}}{R_{o1}C_m}$	$\frac{g_m C_f (1-A_{psr})}{\left(1 + \frac{g_{m1}}{g_{o2}} + \frac{g_{m2} g_{mcf}}{g_{o1} g_{o2}} C_{cf}\right)}$	$\frac{1}{R_{o1}(C_m + 2C_q)}$	$\frac{g_{o1} g_{o3} g_{out} (1-A_{psr}) (1+g_{mp} r_{ds}) (1+M \frac{g_{mps}}{g_{o3}})}{(N g_{m2} g_{mp} + M g_{mps} g_{out}) C_m}$	$\frac{1-A_{psr}}{R_{o2}C_{qd}}$
$\omega_{z2,psr}$	$\frac{1}{R_{o2}C_{qd}}$	-	$\frac{1-A_{psr}}{R_{o2}C_{qd}}$	-	-
$\omega_{p1,psr}$	$\frac{\beta g_{m1}}{C_m}$	$\frac{g_{m2}}{C_{qd}}$	$\frac{\beta g_{m1}}{C_m}$	$\frac{\beta g_{m1}}{C_m}$	$\frac{\beta g_{m1} g_{m2}}{g_{o1} C_m}$
$\omega_{p2,psr}$	$\frac{g_{m2}}{C_{qd}}$	-	$\frac{g_{m2}}{C_{qd}}$	-	-
A_{PSR}^1	-0.12/-0.20	1.36/1.43	0.92/0.96	0.68/1.00	1.29/1.36

¹ Results for $I_L = 100\mu\text{A}/50\text{mA}$

to the effect of the compensation capacitor C_Q as shown in Table 4.3 ($\omega_{z1,psr}$). The transimpedance topology has very good low-frequency PSR at light loads due its high DC loop gain. At heavy loads, the low-frequency PSR is significantly reduced due to its low DC loop gain. This topology has low PSR bandwidth since its $\omega_{z1,psr}$ is placed at very low-frequencies. The differentiator architecture has poor PSR low-frequency performance due to its low DC loop gain. Moreover, its PSR bandwidth is limited due to the large output impedance of the EA and the gate capacitance of the pass transistor.

4.4 Experimental Results

For comparison, we select at least one representative architecture from each of the three groups (Advanced Compensation, Load Transient, and PSR). To compare each topology on the same basis, [18], [23]-[26] (Figure 4.1(a), Figure 4.1(b), Figure 4.4(c), Figure 4.2(b), and Figure 4.2(a)) architectures were designed in the same technology and with the common design specifications shown in Table 4.4. [18] was designed in $0.5\mu\text{m}$ CMOS process and its UGF was approximately 600 kHz. [23]-[26] were designed in $0.35\mu\text{m}$ CMOS process and [23], [24], and [26] have UGFs < 850 kHz. Thus, designing [18], [23], [24], and [26] for an approximately 500 kHz in $0.5\mu\text{m}$ CMOS would not significantly degrade their performance. [25] was originally designed for an UGF between 2 MHz and 10 MHz and hence its transient response might be degraded by reducing its UGF. In terms of the input voltage, all the architectures should be able to operate properly with 3V.

These common design specifications help to reveal the advantages and disadvantages of the five CL-LDO regulator topologies based on their compensation scheme and error amplifier topology. For example, having the same pass transistor dimensions helps to compare stability, transient, and quiescent current since the capaci-

Table 4.4: Targeted design specifications for the CL-LDO regulators

Parameter	Value
V_{IN}	3.0V
V_{OUT}	2.8V
V_{REF}	1.4V
Loop UGF	500kHz
R_{F1}, R_{F2}	100k Ω each (on chip)
Pass Transistor Dimensions	W=36mm, L=0.6 μ m
Technology	0.5 μ m CMOS

tance at the gate of the pass transistor determines the location of the pole and slew rate at that node, and the error amplifier's quiescent current. Moreover, having the same pass transistor dimensions, V_{IN} , and V_{OUT} helps to evaluate the CL-LDO regulator power supply rejection because all the topologies would have the same g_{ds} . In addition, having the same R_{F1} , R_{F2} , V_{OUT} , V_{REF} , and loop UGF helps to normalize noise performance, as the difference between all the topologies are given by the error amplifier noise.

The CL-LDO regulators [18], [23]-[26] were compared in terms of load and line regulation, load and line transient, power supply rejection, quiescent power consumption, maximum tolerable C_L not causing instability, and total on-chip compensation capacitance. Table 4.5 summarizes the performance highlights of all topologies.

4.4.1 Quiescent Current and Stability

From Table 4.5, it can be seen that the transimpedance architecture consumes the lowest quiescent current at $I_L=100\mu$ A where is most critical. This topology uses an adaptive biasing scheme which allows good current efficiency across the entire current range. Also, from Table 4.5, we observe that the Damping Factor and Q-reduction topologies require the largest total on-chip compensation capacitance while the differentiator topology requires the smallest amount to have a UGF of 500kHz

Table 4.5: Measurement performance summary of the designs in 0.5 μ m CMOS technology

Topologies	Damping Factor [18]	Q-Reduction [23]	Voltage Subtractor [24]	Transimpedance [25]	Differentiator [26]
Quiescent Current(μ A) ¹	63/60	64/60	80/100	46 /170	78/80
Total On-chip C_C (pF)	8	7	2.8	2.7	1.2
Maximum C_L (pF)	180	190	610	450	1500
Load Transient $\Delta V_{out}(V)$ ²	1.026/0.650	1.134/0.325	1.207/0.345	0.962/0.289	1.207/0.281
Load Transient Settling (μ s)	1.20/3.09	4.23/1.54	1.73/1.56	1.04/3.56	0.80/1.34
Load Regulation (mV/mA)	0.760	0.721	0.842	0.862	0.902
EA DC Gain (dB) ^{1,3}	79/80	85 / 87	71/63	80/46	51/53
PSR@50mA (dB) ⁴	-52/-50/-27	-63/-45/-20	-48/-47/-26	-46/-26/-7	-53/-36/-16
PSR@100 μ A (dB) ⁴	-54/-52/-38	-66/-48/-26	-82/-62/-39	-50/-31/-11	-49/-42/-22
PSR@100 μ A at DC (dB) ^{3,5}	72/70	88/88	84/83	91/89	57/63
Line Transient (mV)	144/271	264/241	76/93	419/496	428/209
Line Regulation (V/V)	0.018	0.001	0.002	0.001	0.003
Output Noise SD at 100kHz (nV/\sqrt{Hz}) ³	90	100	190	130	140
Integrated output noise (μV_{rms}) ³	44	60	106	79	84
FOM_1 (ps)	0.246	0.272	0.386	0.177	0.377
FOM_2	8.73	17.91	1.59	8.47	0.85

¹ Results for $I_L=100\mu$ A/50mA.² Worst voltage dip/surge for a load step from 100 μ A to 50mA / 50mA to 100 μ A with rise/fall times of 100ns.³ Simulation Results, ⁴ PSR at 1kHz/10kHz/100kHz, ⁵ $V_{in}=3.0V/3.6V$.

and be stable. The differentiator architecture has the smallest amount of on-chip compensation capacitance when compared to the other topologies because of the large capacitance multiplication provided by the gain of the differentiator and the pass transistor. In addition, the differentiator architecture can tolerate the maximum C_L (1500pF) before becoming unstable. This resilience to large capacitive loads stems from capacitive multiplication, which places the dominant pole at extremely low frequencies.

4.4.2 Load Transient/Regulation

Figure 4.10 shows the load-transient response for all architectures. For this test, a load-current step from $100\mu\text{A}$ to 50mA and vice versa with rise and fall times of 100ns was performed. The input voltage V_{IN} and load capacitance C_L were 3V and 10pF, respectively. From Figure 4.10, the voltage subtractor and differentiator

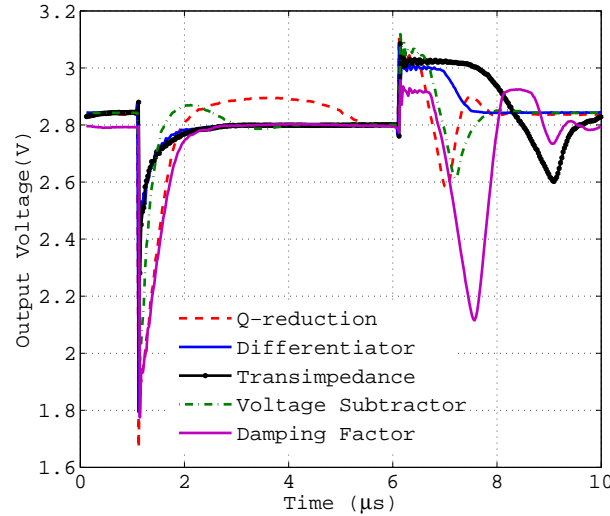


Figure 4.10: Load transient experimental results.

architectures have the largest voltage dips for a current step from $100\mu\text{A}$ to 50mA . The transimpedance architecture has the smallest voltage dip, and the differentiator architecture shows the fastest settling time overall due to their additional dedicated loops to improve the transient response. From simulations, it can be correlated that architectures with smallest/largest voltage dips are the ones that provides the largest/smallest current to drive the gate of the pass transistor. In all the architectures with the exception of the differentiator topology, the maximum current to drive the gate of the pass transistor is determined by the bias current of error amplifier's output stage. For the differentiator topology, the voltage dips can be reduced if the value of C_f capacitor is increased. From Table 4.5, note that the damping factor and Q-Reduction architectures present the best load regulation as well as the highest EA DC gain. In contrast, the Differentiator and Transimpedance architectures exhibit the worst load regulation and the lowest EA DC gain at $I_L = 50\text{mA}$. These observations confirm the relationship between load regulation and EA DC gain shown in (3.5), the higher the EA gain, the better the load regulation and vice versa.

4.4.3 PSR

Figure 4.11 shows the PSR versus frequency for all the architectures at $I_L = 100\mu\text{A}$. The voltage subtractor architecture [24] has the best PSR performance because its A_{PSR} is close to 1 and high loop gain from its three gain stages. The Q-reduction [23] architecture has limited PSR bandwidth because of the compensation capacitor C_Q . Oppositely, the transimpedance [25] and differentiator [26] architectures show the worst PSR performance. The differentiator architecture only has low DC loop gain and its PSR bandwidth is limited due to the large output impedance of the EA and the gate capacitance of the pass transistor. As a result, its PSR is degraded. In this topology, the low-frequency PSR can be improved by increasing

the EA DC gain.

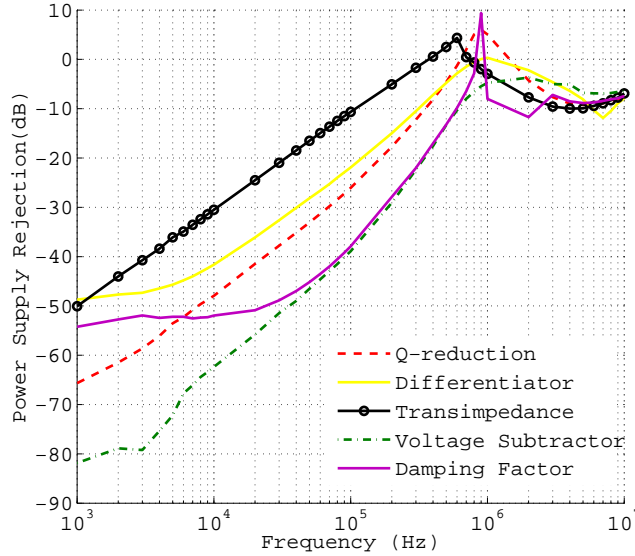


Figure 4.11: PSR measurement results for $I_L=100\mu\text{A}$.

Figure 4.12 shows the PSR versus frequency for all the topologies at $I_L = 50\text{mA}$. As can be seen from Figure 4.12, the Q-reduction technique shows the best PSR from 1kHz to 4kHz due to its high DC loop gain. The damping factor and voltage subtractor topologies present the best PSR from 5kHz to 300kHz. Observe that the PSR of the voltage subtractor degrades at low frequencies for $I_L = 50\text{mA}$ compared to the case when $I_L = 100\mu\text{A}$ because its low-frequency loop gain is lower at $I_L = 50\text{mA}$. The transimpedance and differentiator techniques show the worst PSR performance due to its low DC loop gain at $I_L = 50\text{mA}$.

4.4.4 Line Transient/Regulation

Figure 4.13 shows the line transient response for all architectures. For this test, a voltage step at V_{IN} from 3.0 V to 3.6 V and vice versa with rise and fall times of 600ns

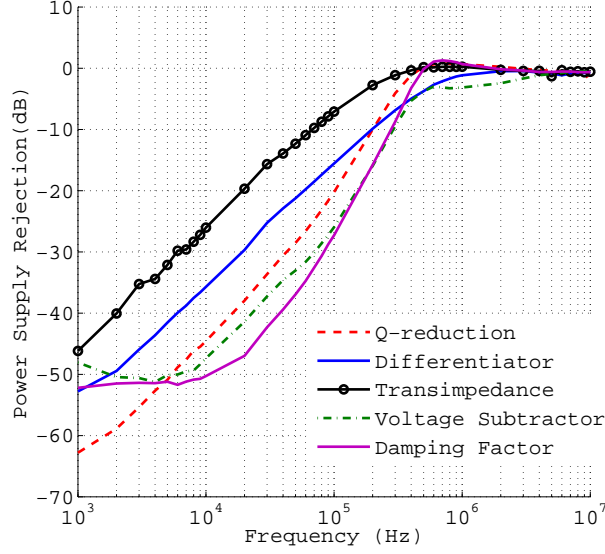


Figure 4.12: PSR measurement results for $I_L=50\text{mA}$.

was performed. The load current I_L and a load capacitor C_L were set to $100\ \mu\text{A}$ and 10pF , respectively. In Figure 4.13, the voltage subtractor architecture has the best line transient response. This result should not be surprising since having good high-frequency PSR typically translates into good line transient as shown in 3.9. For an input voltage step from $3.0\ \text{V}$ to $3.6\ \text{V}$ at the input, the transimpedance technique has the largest voltage surge. For an input voltage step from $3.6\ \text{V}$ to $3.0\ \text{V}$, the transimpedance and differentiator architectures have the largest voltage dips. These results make sense because both techniques have poor high-frequency PSR performance, which typically translates to poor line transient performance as shown in (3.8).

From Table 4.5, note that the transimpedance and Q-Reduction architectures have the best line regulation for $I_L = 100\ \mu\text{A}$ as well as the best PSR at DC. The Differentiator and Damping Factor architectures have the worst line regulation per-

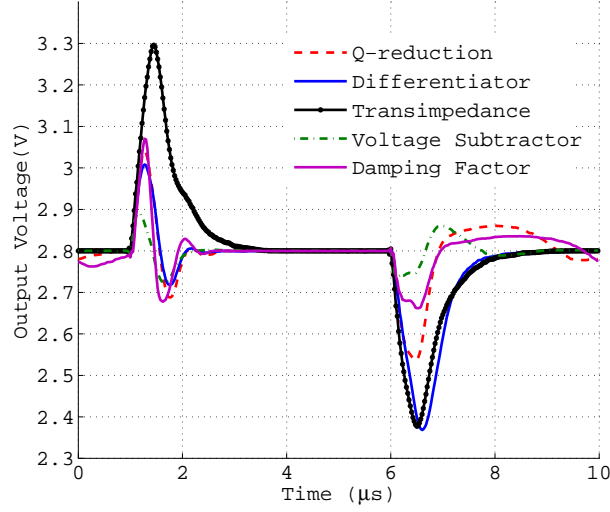


Figure 4.13: Line transient experimental results.

formance and the worst PSR at DC. Thus, these results are consistent since often better PSR corresponds to better line regulation as shown in (3.10).

4.4.5 Noise

Figure 4.14 shows the output noise spectral density simulation results for all the topologies. These results were obtained for a load current of 50 mA and it can be observed that the flicker noise dominates. Table 4.5 summarizes the integrated output noise from 10 Hz to 100kHz and the output noise spectral density at 100kHz results from all the architectures. The error amplifier's first stage transistors are the main noise contributors in the Q-reduction, transimpedance, voltage subtractor, and damping factor architectures and the current amplifier's devices (transistors and resistor) are the main noise contributors of the differentiator topology. In general, as can be seen in Table 4.6, the best (damping-factor/Q-reduction) and worst (voltage subtractor) noise performances correspond to the topologies with the largest and smallest input differential-pairs, respectively. Although the differential-pair dimen-

sions of the differentiator are larger than transimpedance topology; the differentiator architecture has larger output noise because the output noise in the differentiator topology is dominated by g_{mf1} and g_{mf2} .

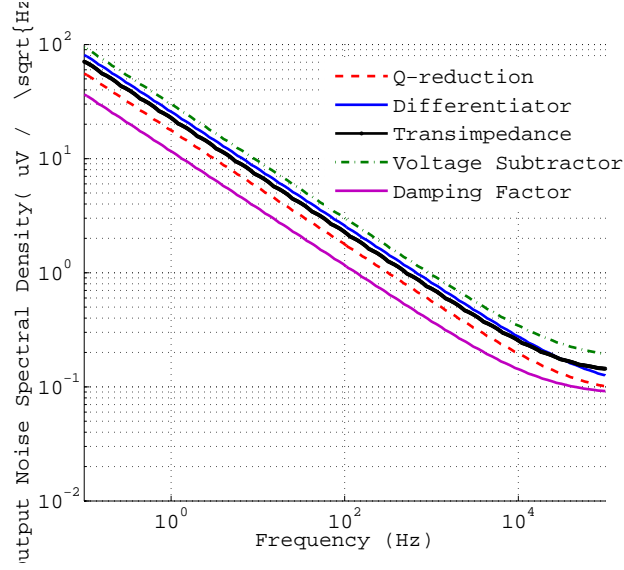


Figure 4.14: Output noise spectral density simulation results.

To compare the LDO regulators, we use the following figure of merit (FOM) [35]:

$$FOM_1 = \frac{C_L \Delta V_{out}}{I_{L,max}} \cdot \frac{I_{q,max}}{I_{L,max}} [ps] \quad (4.3)$$

where $C_L = 10\text{pF}$ and $I_{q,max}$ and $I_{L,max}$ are the maximum quiescent and load current, respectively. The smallest FOM_1 indicates the best regulator. To include the contribution of the PSR, maximum C_L , and total on-chip compensation capacitance C_{cm} , we propose an alternative figure of merit FOM_2 :

$$FOM_2 = \frac{C_{cm}}{C_{L,max}} \cdot \frac{\Delta V_{out}}{V_{out}} \cdot \frac{I_{q,max}}{I_{L,max}} \cdot 10^{(PSR(dB)/20)} \cdot 10^7 \quad (4.4)$$

Table 4.6: Differential pair area (W·L) for each selected topology

Architecture	W·L (μm^2)	Integrated output noise (μV_{rms})
Q-reduction	57.60	60
Differentiator	13.32 (1.8/3.6) ¹	84
Transimpedance	8.00	79
Voltage Subtractor	6.44	106
Damping Factor	96.48	44

¹ W·L for (g_{mf1}/g_{mf2}) transistors.

Table 4.7: CL-LDO qualitative features

LDO Topology	Best Performance	Second Best Characteristic
Damping Factor [18]	Heavy load PSR, Low output noise	Light load PSR, Low I_Q Load Transient ΔV_{out}
Q-Reduction [23]	Line regulation, Load regulation	Low output noise, Low I_Q
Voltage Subtractor [24]	Line Transient, Light Load PSR	Heavy Load PSR, Maximum C_L
Transimpedance [25]	Load Transient ΔV_{out} , Line regulation, Low I_Q	Small Compensation Capacitance
Differentiator [26]	Load Transient Settling, Maximum C_L , Small Compensation Capacitance	

For the FOM_2 calculation, we use the PSR at 100kHz for $I_L=50\text{mA}$. The smallest FOM_2 indicates the best regulator. Table 4.7 succinctly summarizes the CL-LDOs regulators [18], [23]-[26] key qualitative characteristics.

4.5 Conclusion

A comparative study of illustrative CL-LDO regulator architectures has been presented. All the architectures were designed using $0.5\mu\text{m}$ CMOS technology and compared in terms of line and load regulation, PSR, line and load transient, total

on-chip compensation capacitance, and quiescent power consumption. There is not a single CL-LDO regulator architecture that outperform all the other for a set of specifications. Trade-offs between the architecture and performance are very much application-dependent. Key design issues for capacitor-less LDO regulators have been addressed.

5. FUNDAMENTALS OF INDUCTOR SWITCHING DC-DC CONVERTERS

5.1 Introduction

Inductor switching DC-DC converters are very important in battery powered applications due to their high efficiency and their capability to generate DC output voltages larger or lower than the input voltage. We will refer to them as DC-DC switching converters for the rest of this dissertation.

In this section, isolated and non-isolated DC-DC switching converters are introduced. Buck converter basics such as operation modes, output filter components selection, and efficiency are also discussed. Some of the main control schemes are introduced and compared. In addition, practical design considerations for the integrated circuit building blocks and printed circuit board in buck converters are included.

5.2 Non-Isolated versus Isolated DC-DC switching converters

DC-DC switching converters can be classified into non-isolated and isolated topologies. The difference between both topologies stems from the fact that in isolated architectures, DC isolation between the input and output is typically achieved with a transformer [3]. In some isolated topologies (i.e., flyback converter), multiple DC output voltages can be obtained by adding additional secondary windings and circuitry. Moreover, for large step-up or step-down conversion ratios, very good performance can be achieved [3]. Nevertheless, isolated architectures are typically more expensive and occupy more area than non-isolated topologies due to the transformer.

Some examples of non-isolated topologies are: buck, boost, buck-boost, cuk, sepic, and zeta converters. These converters consist of one switch, one diode, inductors, and capacitors. Buck, boost, and buck-boost are implemented with one

inductor while cuk, sepic, and zeta converters require two inductors [3]. These components are interconnected in different ways to generate an output voltage smaller or larger than the input voltage. For example, a buck converter generates a smaller output voltage than input voltage, while a boost converter generates a larger output voltage than the input. Boost, cuk, sepic, and zeta converters can generate output voltages smaller or larger than the input voltage. Isolated topologies include: flyback, forward, push-pull, half-bridge, and full-bridge converters [3].

5.3 Buck Converter Operation

The buck converter is a step down DC-DC converter, and it is probably the most popular DC-DC converter today. One common application of buck converters is in chargers for portable electronics such as cellular phones, MP3 players, electronics book readers, etc. For example, in cellular phone car chargers, they are used to step down with high efficiency from 12V car's battery to 5V to charge the cellular phone. This task can be also performed using a linear regulator (see section 3) but with an efficiency smaller than 50 %.

The buck converter can be classified as asynchronous and synchronous based on how the power stage is implemented. An asynchronous buck converter consists of a MOSFET (M_p), a diode (D_n), an inductor (L), and a capacitor (C) as shown in Figure 5.1 (a). The synchronous topology is almost identical to the asynchronous one, but the diode is replaced with a NMOS transistor (M_n) as shown in Figure 5.1 (b). The synchronous topology typically presents higher efficiency at heavy loads than the asynchronous topology because the losses due to the on-resistance of M_n are typically smaller than the ones of diode D_n [45]. Nevertheless, the synchronous topology requires a more complicated drive circuitry to avoid turning on both transistors at the same time [46]. Further details will be provided later in this section.

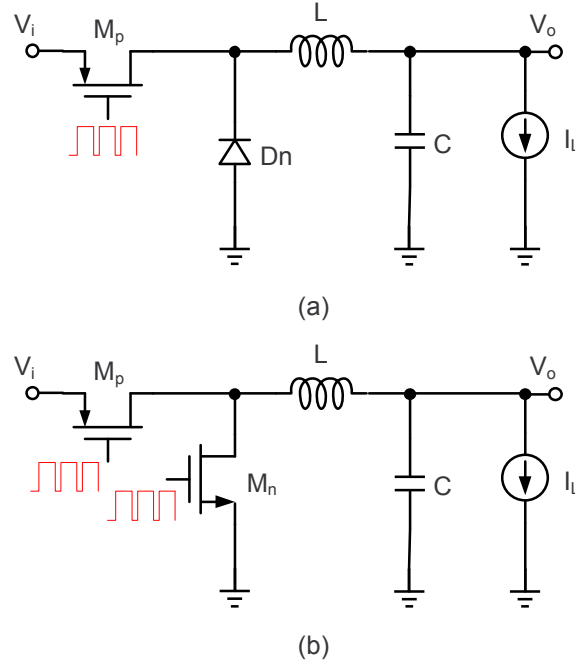


Figure 5.1: Buck converter in (a) asynchronous (b) synchronous.

The operation of buck converters can be classified under two categories: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM operation, the current flowing through the inductor is continuous during a switching period as shown in Figure 5.2(a). In DCM operation, the current flowing through the inductor clips at zero during a portion of the switching period as shown in Figure 5.2(b). DCM operation typically occurs for large inductor current ripple, small load current, and current-unidirectional switches [3]. In CCM, the output voltage of the buck converter can be expressed as:

$$V_{OUT} = D \cdot V_{IN} \quad (5.1)$$

where V_{IN} and D are the input voltage and duty cycle, respectively. In DCM, the

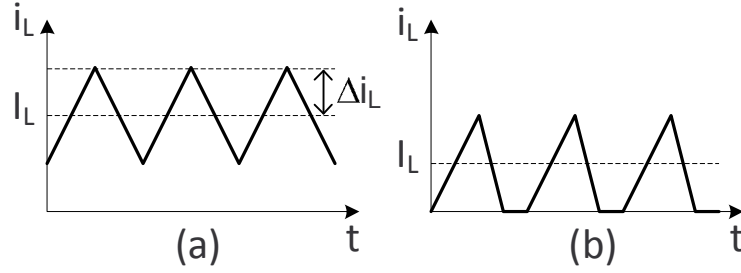


Figure 5.2: Buck converter operating in (a) continuous conduction mode (CCM) (b) discontinuous conduction mode (DCM).

output voltage of the buck converter can be expressed as [3]:

$$V_{OUT} = V_{IN} \cdot \frac{2}{1 + \sqrt{\frac{4K}{D^2}}} \quad (5.2)$$

where

$$K = \frac{2L}{R_L T_s}$$

Equation (5.2) is valid for $K < K_{crit} = (1 - D)$. Figure 5.3 shows $M(D, K)$ versus D for different K values, where $M(D, K) = V_{OUT}/V_{IN}$. Notice that for $K < K_{crit}$ the effect of DCM operation causes V_{OUT} to increase when compared with $K = 2K_{crit}$ (CCM case).

Table 5.1 summarizes the main advantages and disadvantages of a buck converter operating in CCM and DCM for constant switching frequency. As can be seen, a buck converter operating in CCM achieves smaller ripple, lower output impedance, higher efficiency, and lower peak current than in DCM for a given load current [3]. However, a buck converter operating in DCM behaves as a single-pole system which simplifies the compensation. Area can be also reduced in DCM operation since the required output filter inductance value is smaller than in CCM at the expense of

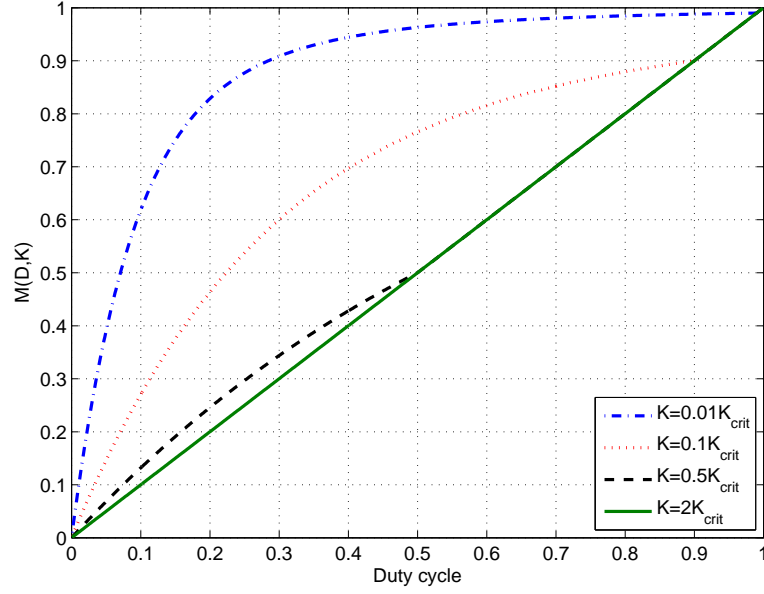


Figure 5.3: Buck converter's voltage conversion ratio (V_{OUT}/V_{IN}) versus D for different K values.

Table 5.1: CCM versus DCM		
	Advantages	Disadvantages
CCM	V_{OUT} is load independent, smaller ripple, lower output impedance, higher efficiency, Lower peak current	Larger inductance (L), second-order system
DCM	Smaller inductance (L), first-order system	V_{OUT} is load dependent, higher output impedance, lower efficiency, larger ripple, higher peak current

larger ripple.

5.4 Buck Converter Output Filter Component Selection

5.4.1 Output Inductor

The value of the output filter inductance is typically chosen based on the current ripple specifications. Assuming CCM operation, the output filter inductance can be expressed as [3],

$$L = \frac{D \cdot (V_{IN} - V_{OUT})}{2\Delta i_L f_s} \quad (5.3)$$

where Δi_L and f_s are the peak current ripple and switching frequency, respectively. Inductors are not ideal components with only inductance, they have a parasitic DC resistance (DCR) that affects the DC-DC converter performance. This parasitic resistance degrades the efficiency performance, which will be demonstrated later in section 5.5.1. Nevertheless, it can be used to sense the inductor's current in buck converters implemented with current mode control as will be shown later in section 5.6.2.4 [47]. Assuming a unidirectional switch, $L < ((1 - D) \cdot R_L)/(2f_s)$ is required to operate in DCM.

5.4.2 Output Capacitor

The value of the output capacitor is usually determined by the voltage dips/surges (ΔV_{OUT}) specifications during load transient (ΔI_L) and output voltage ripple specifications (Δv_{out}) in steady-state. Figure 5.4 shows the output voltage and load current waveforms during a load transient event.

Assuming CCM operation, the value of the output capacitor based on output voltage ripple is given by [3]:

$$C = \frac{\Delta i_L}{8f_s \Delta v_{out}} = \frac{D(V_{IN} - V_{OUT})}{16f_s^2 L \Delta v_{out}} \quad (5.4)$$

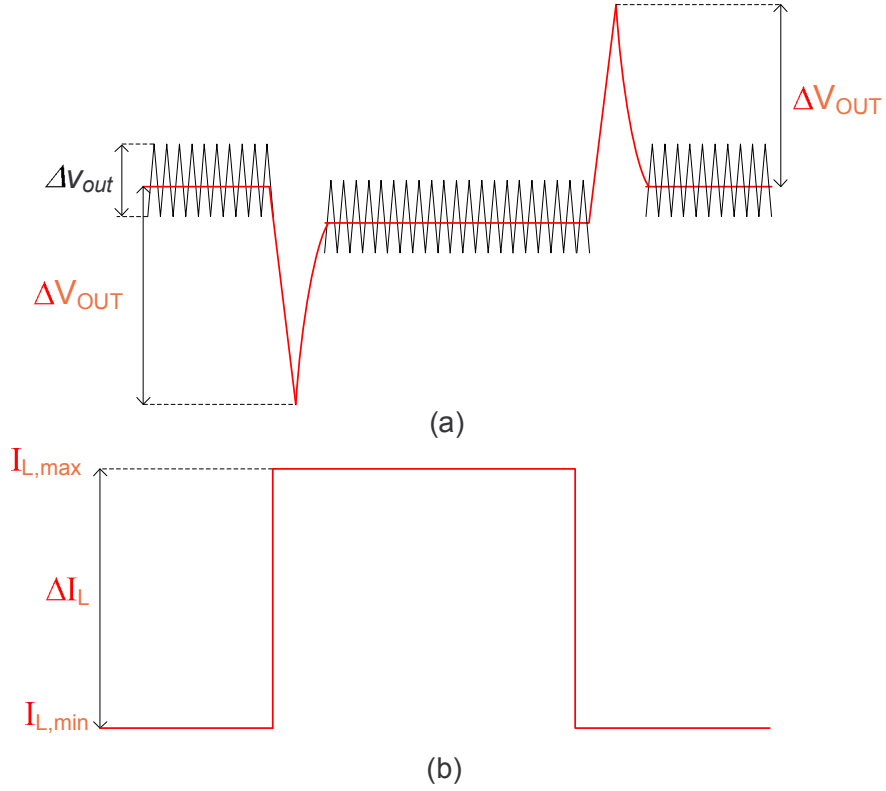


Figure 5.4: Buck converter (a) output voltage and (b) load current waveforms during a load transient event.

The voltage dip/surges can be estimated using the equivalent circuit for the buck converter shown in Figure 5.5. where it is assumed that the feedback loop does not react fast enough to a sudden load change and as a result, the output impedance is determined by the output capacitor. Hence, the voltage dip/surge (ΔV_{OUT}) during load transient can be approximated as:

$$\Delta V_{OUT} \cong \Delta V_{ESR} + \Delta V_C = \frac{\Delta I_L \cdot t_1}{C} + R_{ESR} \cdot \Delta I_L \quad (5.5)$$

where t_1 and ΔI_L are the loop reaction time and the load current step, respectively. R_{ESR} represents the equivalent series resistance of the capacitor. Time t_1 is a function

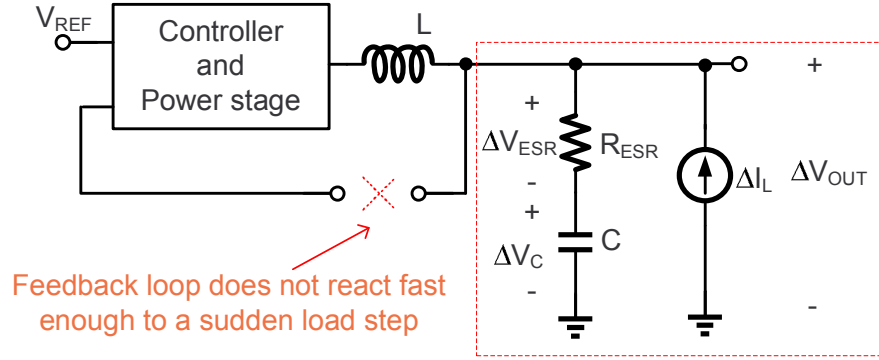


Figure 5.5: Equivalent buck converter for load transient analysis.

of the crossover frequency or unity gain frequency of the loop assuming that the system is not slew rate limited. From (5.5), the value of the output capacitor based on load transient specifications can be written as:

$$C = \frac{\Delta I_L \cdot t_1}{\Delta V_{OUT} - \Delta I_L \cdot R_{ESR}} \quad (5.6)$$

Hence, the larger of the two calculated capacitor values using (5.4) and (5.6) must be chosen to meet both voltage ripple and load transient specifications. For instance, for $V_{IN} = 1.8$ V, $V_{OUT} = 0.9$ V, $L = 4.7$ μ H, $f_s = 1$ MHz, $R_{ESR} = 20$ m Ω , $f_c = 100$ kHz ($t_1 \approx 1/(2\pi f_c)$), $\Delta v_{out} = 4$ mV, and $\Delta V_{OUT} = 100$ mV. Finally, (5.4) and (5.6) yield 1.5 μ F and 5.7 μ F, respectively. Hence, an output capacitor of 5.7 μ F or closest standard capacitor value should be chosen to meet both specifications.

5.5 Efficiency in Buck Converters

The buck converter can ideally provide an efficiency of 100%. Nevertheless, losses due to non-ideal switches and passives components degrade the efficiency. Moreover, the required power to operate the controller reduces the efficiency even further. These

power losses can be classified as: conduction (P_c), dynamic (P_{dyn}), gate drive (P_{gdrv}), quiescent (P_Q), body diode (P_{body}), and short circuit (P_{short}) losses as shown in Figure 5.6.

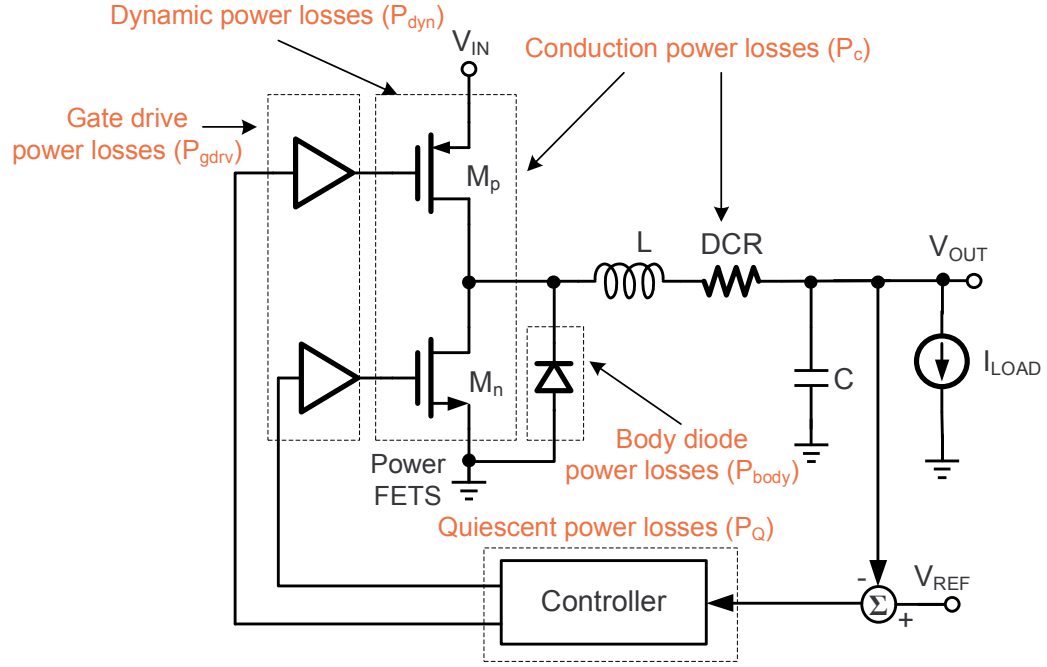


Figure 5.6: Buck converter power losses sources.

The total power losses are given by:

$$P_{losses} = P_c + P_{dyn} + P_{gdrv} + P_{body} + P_Q + P_{short} \quad (5.7)$$

5.5.1 Conduction Power Losses

The conduction power losses P_c in CCM for a synchronous buck converter are given by:

$$P_c = D \cdot R_{on,p} \cdot I_{L,rms}^2 + (1 - D) \cdot R_{on,n} \cdot I_{L,rms}^2 + DCR \cdot I_{L,rms}^2 \quad (5.8)$$

where

$$I_{L,rms} = I_{L,avg} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_L}{I_{L,avg}} \right)^2} \quad (5.9)$$

Resistors $R_{on,p}$ and $R_{on,n}$ represent the on-resistances of the PMOS (M_p) and NMOS (M_n) power transistors (see Figure 5.1 (b)), correspondingly. The first term of (5.8) represents the losses due to the PMOS transistor; the second term represents the loss due to the NMOS transistor, and the third term represents the loss due to the parasitic resistance of the inductor. For a typical inductor current ripple of $\Delta i_L = 0.2 \cdot I_{L,avg}$, the actual conduction losses increase only by 1.33%; hence, $I_{L,avg} \cong I_{L,rms}$ for small Δi_L . As can be seen from (5.8), the conduction losses can be reduced if the value of $R_{on,n}$, $R_{on,p}$, and DCR are minimized. The conduction losses are particularly dominant at heavy loads (large I_L). In the case of an asynchronous buck converter, the conduction power losses can be written as:

$$P_c = D \cdot R_{on,p} \cdot I_{L,avg}^2 + (1 - D) \cdot V_{diode} \cdot I_{L,avg} + DCR \cdot I_{L,avg}^2 \quad (5.10)$$

where V_{diode} represents the forward bias voltage of the diode. Notice that using a diode with small forward bias voltage such as a Schottky diode reduces the conduction losses [45].

When operating with low duty cycle at heavy loads, the low side device (M_n or

Dn) is conducting for a larger portion of the period than the high side device (M_p); as a result, its power losses are critical. In this condition, a synchronous buck converter typically achieves higher efficiency than an asynchronous buck converter because the losses due to the on-resistance of M_n are smaller than the ones of Dn [45]-[46]. On the other hand, when operating at high duty cycles and light loads, an asynchronous buck converter may provide higher efficiency than a synchronous one because the losses due to switching of the low-side power transistor (M_n) and associated driving circuitry may be larger dominate than the diode ones [46].

5.5.2 Dynamic Power Losses

The dynamic power losses are due to switching behavior of the power transistor [45]-[46] and are given by:

$$P_{dyn} = 0.5 \cdot V_{IN} \cdot I_{L,avg} \cdot (t_r + t_f) \cdot f_s \quad (5.11)$$

where t_r and t_f are the duration of the turn on and off transitions of the MOSFET, respectively. In [48], a buck converter with an auto-selectable-frequency technique is proposed. This technique reduces f_s at light loads to improve the efficiency by 27%.

5.5.3 Gate Drive Power Losses

The gate drive power losses are typically critical at light loads and determined by the required power to drive the gate of the power transistor, and they are given by [49]:

$$P_{gdrv} = C_{GATE} \cdot f_s \cdot V_{GS}^2 \quad (5.12)$$

where C_{GATE} and V_{GS} are the gate capacitance and gate-to-source voltage of the MOSFET, respectively. These losses can be minimized by reducing C_{GATE} , f_s , and/or V_{GS} . In low power applications, V_{GS} is approximately V_{IN} .

A buck converter with a gate charge modulation and recycling technique is proposed in [50]. This topology reduces the drive loss and as result improves the efficiency by 5 % at light loads. In [51], a buck converter is proposed to reduce the switching losses by reducing the effective input voltage supply at light loads. This technique reduces both dynamic and gate drive power losses. An efficiency improvement of up to 20 % is achieved at light loads.

5.5.4 Body Diode Power Losses

In a synchronous buck converter, a non-overlapping time (t_{no}) is added to the power FETs driver to avoid shoot-through current. Nevertheless, during the non-overlapping time when both transistors (M_p and M_n) are off, the body diode of M_n is conducting. The power loss due to this body diode is given by [45]:

$$P_{body} = 2 \cdot V_{body} \cdot I_{L,avg} \cdot t_{no} \cdot f_s \quad (5.13)$$

where V_{body} is the forward bias voltage of the body diode. For example, for $I_{avg} = 500$ mA, $f_s = 1$ MHz, $V_{body} = 0.7$ V, and $t_{no} = 5$ ns, the power loss due to the body diode is 3.5 mW.

5.5.5 Quiescent Power Losses

The quiescent power loss (P_Q) is basically the minimum required power by the controller to operate properly and is given by [46]:

$$P_Q = V_{IN} \cdot I_Q \quad (5.14)$$

where I_Q is the quiescent current. P_Q is particularly important at very light loads or idle mode.

5.5.6 Short Circuit Power Losses

Short circuit power losses P_{short} occur when the high side (M_p) and low side (M_n) power transistors in a synchronous buck converter are ON at the same time. The power transistors may be damaged if this event occurs. The short circuit current is greatly minimized using a non-overlapping circuit to avoid the occurrence of both transistors conducting at the same time. The non-overlapping time needs to be large enough such that the power loss due to the short circuit current is absent but small enough such that the power loss due to the time that the body diode of the low-side power transistor conducts does not affect the efficiency performance.

Then, efficiency is given by:

$$\eta = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_{losses}} \quad (5.15)$$

where P_i and P_o are the input and output power losses, respectively. Typically, the efficiency is higher at heavy loads and lower at light loads.

5.6 Main Control Schemes

Buck converter voltage regulators operate in closed loop fashion to minimize the effect of load perturbations and/or input voltage variations, which could affect the output voltage [3]. However, this closed loop operation makes the buck converter stability a concern. In this section, we discuss the main control schemes: voltage mode pulse width modulation (PWM), current mode PWM, hysteretic control, sliding mode control, and digital control.

5.6.1 Voltage Mode PWM Compensation

Figure 5.7 shows the closed loop block diagram of a voltage mode PWM buck converter which includes a compensator, a carrier signal generator, a comparator, a

power stage, and an output filter.

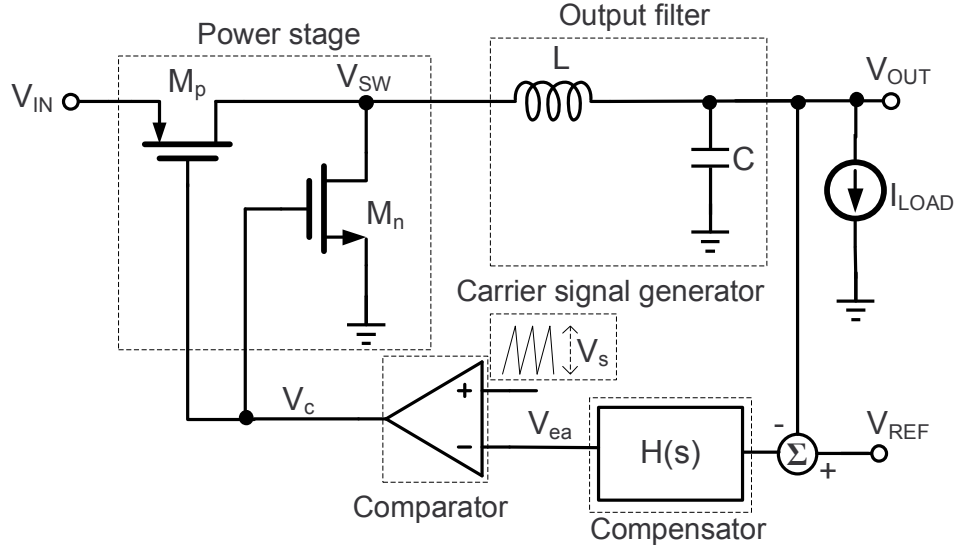


Figure 5.7: Block diagram of a buck converter with voltage mode PWM control.

This system operates as follows: If V_{ea} is larger than the carrier signal voltage (e.g. $V_{OUT} < V_{REF}$), then V_c turns on and off M_p and M_n , respectively. This effect causes the inductor current to increase and as a result V_{OUT} also increases. The opposite effect would occur if V_{ea} is smaller than the carrier signal voltage (e.g., $V_{OUT} > V_{REF}$).

When analyzing the stability of the loop, the combination of the carrier signal generator, comparator, and power stage is typically referred to as the modulator, and its gain is often assumed to be constant (V_{IN}/V_s) [52]-[53].

Figure 5.8 shows the output filter including the parasitic resistances of the capacitor and inductor.

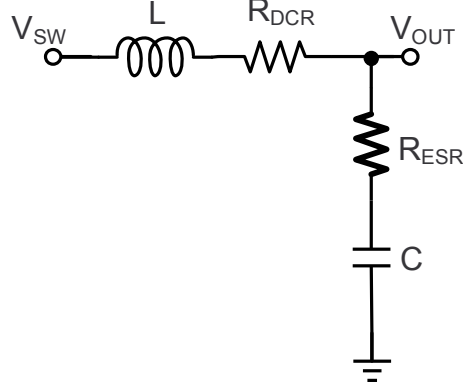


Figure 5.8: Buck converter's output filter with parasitics.

The transfer function of the output filter is given by:

$$F(s) = \frac{V_{OUT}(s)}{V_{SW}(s)} = \frac{sCR_{ESR} + 1}{LCs^2 + (R_{ESR} + R_{DCR})Cs + 1} \quad (5.16)$$

Hence, the overall open loop transfer function of the buck converter without compensation block is given by:

$$H(s)_{open-loop} = \frac{V_{IN}}{V_s} \cdot \frac{sCR_{ESR} + 1}{LCs^2 + (R_{ESR} + R_{DCR})Cs + 1} \quad (5.17)$$

$$H(s)_{open-loop} = \frac{V_{IN}}{V_s} \cdot \frac{\frac{s}{\omega_z} + 1}{\frac{s^2}{\omega_o^2} + \frac{1}{\omega_o Q}s + 1} \quad (5.18)$$

where

$$\omega_o = \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_{ESR}C}, \quad Q = \frac{1}{R_{ESR} + R_{DCR}} \sqrt{\frac{L}{C}} \quad (5.19)$$

Because the term $(R_{ESR} + R_{DCR})C$ is usually small, the loop can be approximated to have a double pole located at $\omega_o = \omega_{LC} = 1/(\sqrt{LC})$ and a zero at $\omega_z = \omega_{ESR} = 1/(R_{ESR}C)$. Figure 5.9 depicts the Bode plot of the open loop transfer function.

The gain at low-frequencies is given by the modulator gain (V_{IN}/V_s). After ω_{LC} ,

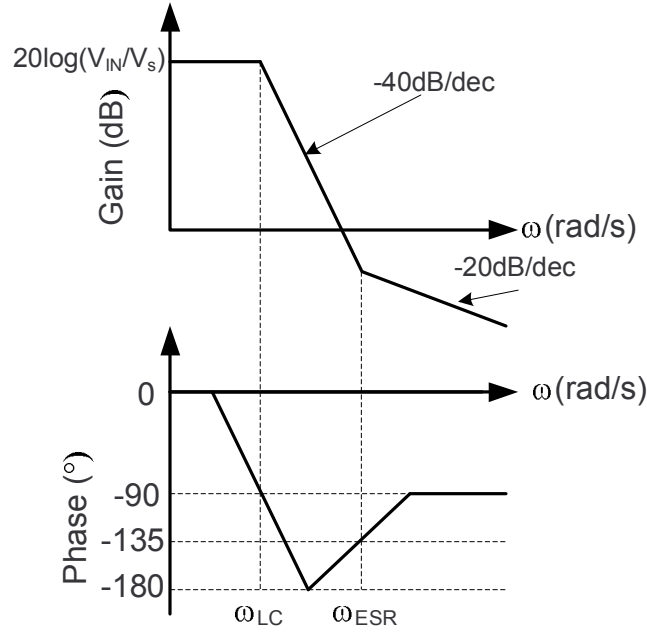


Figure 5.9: Open loop Bode plot without compensation block.

the gain starts to roll off at -40dB/decade and the phase quickly reaches -180°. If R_{ESR} is very small, which is typically the case for load transient and output ripple voltage specifications, ω_{ESR} is located at high frequencies and it does not help to compensate the loop. Thus, this system has poor phase margin and low DC-gain. A compensator is necessary to boost the loop phase margin to counteract the effect of the output filter's complex poles located at $f_{LC} = 1/(2\pi\sqrt{LC})$ and increase the loop gain.

5.6.1.1 Type-I Compensation

A Type-I voltage mode compensator (an integrator) can be used to stabilize the loop. This compensation scheme is simple since it only requires a resistor, a capacitor, and an amplifier. However, the loop crossover frequency must be smaller than f_{LC} to guarantee good phase margin; and as a result, poor transient response is expected. Figure 5.10 shows a possible implementation for a Type-I compensator.

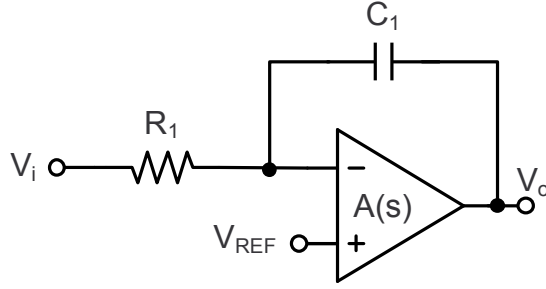


Figure 5.10: Type-I compensator implementation.

The transfer function of this network assuming an ideal amplifier is given by:

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1}{R_1 C_1 s} \quad (5.20)$$

This transfer function has one low-frequency pole. The transfer function of the system for a non-ideal amplifier $A(s) = A_o / (1 + s/\omega_{p0})$ is given by:

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{A_o}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (5.21)$$

where

$$\omega_{p1} \cong \frac{1}{A_o R_1 C_1}, \quad \omega_{p2} \cong \omega_{p0} A_o = GB \quad (5.22)$$

Parameters A_o , ω_o , and GB are the DC gain, dominant pole, and gain bandwidth product of the amplifier. Figure 5.11 illustrates the Bode plot for (5.21). Notice that Figure 5.11 is not drawn at scale and ω_{p2} typically occurs at high frequencies in a good design.

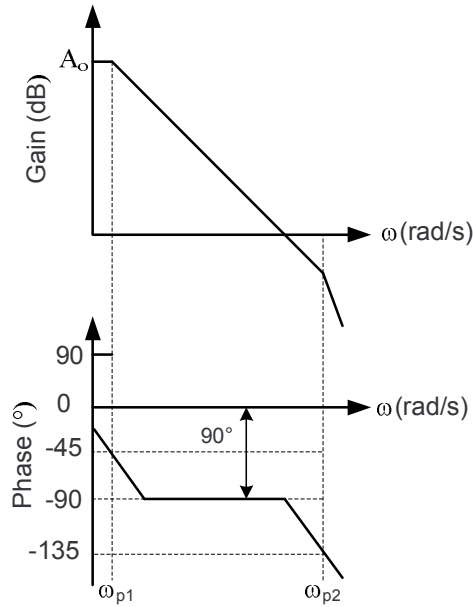


Figure 5.11: Type-I compensator Bode plot.

5.6.1.2 Type-II Compensation

A Type-II voltage mode compensator is another option in buck converters; however, the equivalent series resistance (R_{ESR}) of the output filter capacitor must be relatively large to generate a low-frequency zero, given by $f_{ESR} = 1/(2\pi R_{ESR}C)$, to

provide phase boost to achieve stability. Figure 5.12 shows a Type-II compensator implementation. The transfer function of this network assuming an ideal amplifier

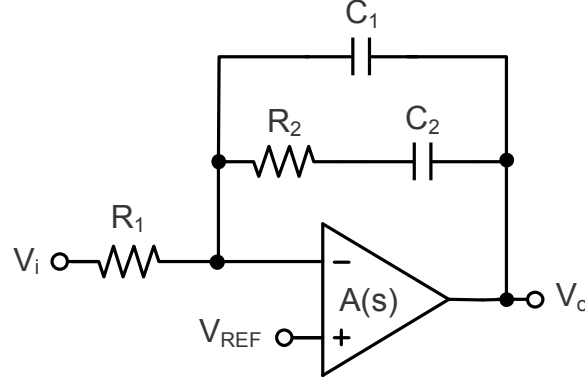


Figure 5.12: Type-II compensator implementation.

is given by:

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{\frac{s}{\omega_{z1}} + 1}{R_1 (C_1 + C_2) s \left(\frac{s}{\omega_{p2}} + 1 \right)} \quad (5.23)$$

where

$$\omega_{z1} = \frac{1}{R_2 C_2}, \quad \omega_{p2} = \frac{1}{R_2 (C_1 C_2) / (C_1 + C_2)}$$

This transfer function has one low-frequency zero, one low-frequency pole, and one high-frequency pole. The transfer function of the system for a non-ideal amplifier $A(s) = A_o / (1 + s/\omega_{p0})$ is given by:

$$H(s) = \frac{V_o(s)}{V_i(s)} = -A_o \cdot \frac{\frac{s}{\omega_{z1}} + 1}{\left(\frac{s}{\omega_{p1}} + 1 \right) \cdot \left(\frac{s}{\omega_{p2}} + 1 \right) \cdot \left(\frac{s}{\omega_{p3}} + 1 \right)} \quad (5.24)$$

where

$$\omega_{z1} = \frac{1}{R_2 C_2}, \quad \omega_{p1} = \frac{1}{A_o R_1 (C_1 + C_2)}, \quad (5.25)$$

$$\omega_{p2} = \frac{1}{R_2 (C_1 C_2) / (C_1 + C_2)}, \quad \omega_{p3} = \omega_o A_o = GB \quad (5.26)$$

Figure 5.13 illustrates the Bode plot for Type-II compensation network with non-ideal amplifier. In Figure 5.13, it was assumed that ω_{p3} was located at high frequencies and its effect was neglected. There are different approaches on where to place the low-frequency zero and high frequency pole [52]-[53]. For instance, the procedure suggested in [52], places the zero at half f_{LC} and the high frequency pole at $f_s/2$. One issue with this compensation is that the R_{ESR} may vary significantly

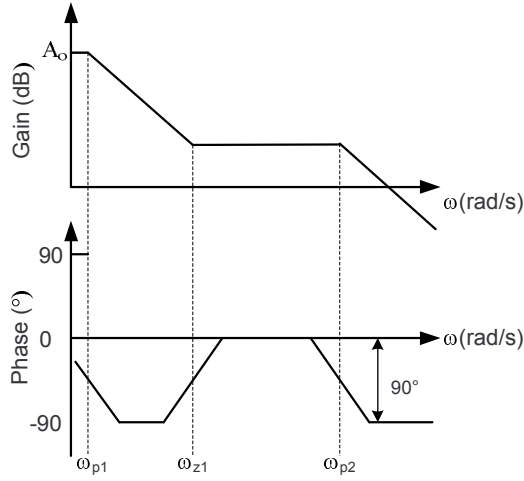


Figure 5.13: Type-II compensator Bode plot.

over temperature, and stability could be degraded. Moreover, having a large R_{ESR} would increase the output voltage ripple as well as the amplitude of the voltage dips and surges during load transient events as shown in (5.6).

5.6.1.3 Type-III Compensation

Type-III compensation is typically used to increase the crossover frequency beyond f_{LC} (but, it is limited to one-fifth of the switching frequency (f_s) due to the sampling effect). Type-III is also used to improve the phase margin in applications where fast transient response and an output filter capacitor with small R_{ESR} are required [54]. The conventional Type-III compensation network shown in Figure 5.14 requires three capacitors, three resistors, and an amplifier $A(s)$. The transfer func-

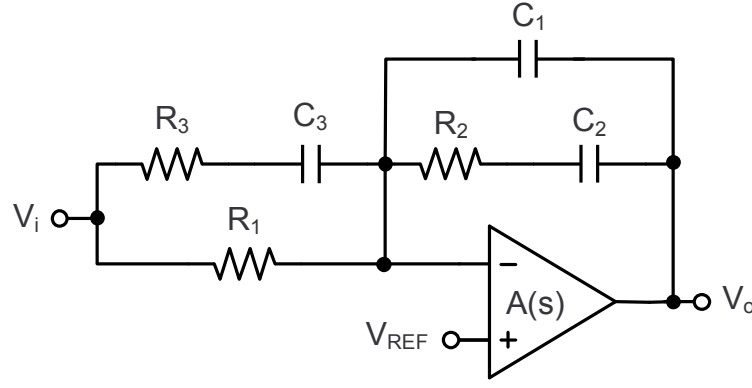


Figure 5.14: Conventional Type-III compensation.

tion of this network assuming an ideal amplifier is given by:

$$H(s)_{Conv} = \frac{V_o(s)}{V_i(s)} = \frac{-\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{R_1(C_1 + C_2)s \cdot \left(\frac{s}{\omega_{p2}} + 1\right) \cdot \left(\frac{s}{\omega_{p3}} + 1\right)}. \quad (5.27)$$

where

$$\omega_{z1} = \frac{1}{R_2 C_2}, \quad \omega_{z2} = \frac{1}{(R_1 + R_3) C_3},$$

$$\omega_{p2} = \frac{1}{R_3 C_3}, \quad \omega_{p3} = \frac{1}{R_2(C_1 C_2)/(C_1 + C_2)}.$$

This transfer function has two low-frequency zeros, one low-frequency pole, and two high-frequency poles. The transfer function of the system for a non-ideal amplifier $A(s) = A_o / (1 + s/\omega_{p0})$ is given by:

$$H(s)_{Conv} = \frac{V_o(s)}{V_i(s)} = A_o \cdot \frac{-\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p2}} + 1\right) \cdot \left(\frac{s}{\omega_{p3}} + 1\right) \cdot \left(\frac{s}{\omega_{p4}} + 1\right)}. \quad (5.28)$$

where

$$\omega_{z1} = \frac{1}{R_2 C_2}, \quad \omega_{z2} = \frac{1}{(R_1 + R_3) C_3}, \quad \omega_{p1} = \frac{1}{A_o R_1 (C_1 + C_2)}, \quad (5.29)$$

$$\omega_{p2} = \frac{1}{R_3 C_3}, \quad \omega_{p3} = \frac{1}{R_2(C_1 C_2)/(C_1 + C_2)}, \quad \omega_{p4} = A_o \omega_{p0}. \quad (5.30)$$

Figure 5.15 illustrates the Bode plot of the Type-III compensation network.

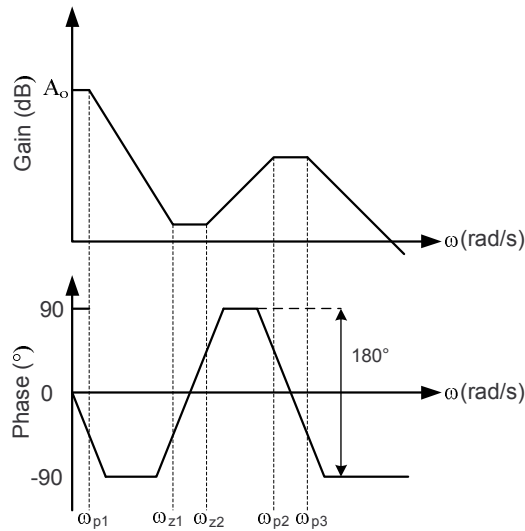


Figure 5.15: Conventional Type-III Bode plot.

In Figure 5.15, it is assumed that ω_{p3} is located at high frequencies, and its effect is neglected. The zeros compensate for the phase lag of the output filter's complex poles. Large capacitors and resistors are often required to generate these low-frequency zeros, and a high-bandwidth amplifier is required to avoid misplacement of the high-frequency poles. There are different approaches on where to place the two low-frequency zeros [52]-[53]. For instance, the procedure suggested in [52] places one zero at f_{LC} and the other one at half f_{LC} . The two high frequency poles, ω_{p2} and ω_{p3} , are placed at $f_s/2$ and f_{ESR} , respectively. The guidelines for placing the poles and zeros in [52] give the following instruction:

1. Select a value for R_1 .
2. Select a gain (R_2/R_1) that shifts the open loop gain up to achieve the desired crossover frequency. This allows the crossover frequency to occur in the frequency range that the Type-III compensator has its second flat gain. This can be achieved using the following equation:

$$R_2 = \frac{f_c}{f_{LC}} \cdot \frac{V_s}{V_{IN}} \cdot R_1 \quad (5.31)$$

3. Calculate C_2 by placing zero f_{z1} at $f_{LC}/2$:

$$C_2 = \frac{1}{\pi R_2 f_{LC}} \quad (5.32)$$

4. Calculate C_1 by placing pole f_{p2} at f_{ESR} :

$$C_1 = \frac{C_2}{2\pi R_2 C_2 f_{ESR} - 1} \quad (5.33)$$

5. Place pole f_{p3} at $f_s/2$ and zero f_{z2} at f_{LC} . This can be accomplished using the

following equations:

$$R_3 = \frac{R_1}{\frac{f_s}{2f_{LC}} - 1} \quad (5.34)$$

$$C_3 = \frac{1}{\pi R_3 f_s} \quad (5.35)$$

5.6.2 Current Mode PWM Compensation

5.6.2.1 Peak Current Mode

Figure 5.16 shows a simplified block diagram of a buck converter with peak current mode control. This compensation scheme has a fast inner loop (current loop) and a

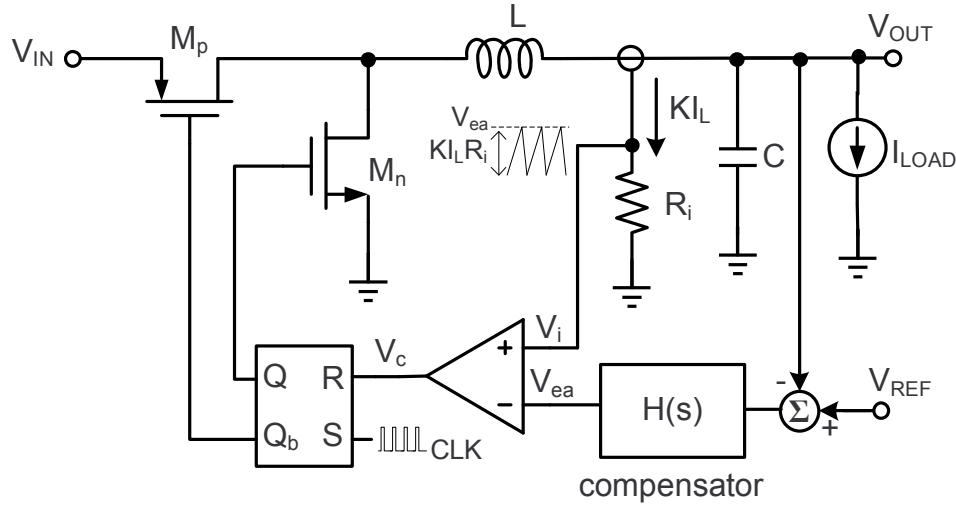


Figure 5.16: Buck converter with peak current mode control block diagram.

slow outer loop (voltage loop). Notice that V_i is proportional to the inductor current, and it generates the carrier signal for PWM.

The operation of this compensation scheme can be described as follows: At the beginning of each cycle the clock signal (CLK) sets the SR-latch ($Q=1$, $Q_b = 0$) to

turn on and off M_p and M_n , respectively. This effect causes the inductor current to increase. When $V_i = V_{ea}$, V_c resets the SR-Latch ($Q=0$, $Q_b = 1$) to turn off and on M_p and M_n , correspondingly. This makes the inductor current to decrease.

One advantage of current mode PWM over the conventional voltage mode PWM is the line transient performance. This is due to the fact that the carrier signal V_i during the on-time of M_p is proportional to V_{IN} (i.e., $V_{IN}-V_{OUT}$) and it provides a pseudo feed-forward path [55].

Another advantage of current mode PWM over voltage mode PWM is that the output filter transfer function behaves as a single pole ($1/(R_L C)$) in the region of interest [3]. This simplifies the compensation block ($H(s)$) when compared with Type-III compensation scheme in voltage mode. In current mode, an $H(s)$ implementation with one zero can stabilize the loop. A typical implementation of the compensator is shown in Figure 5.17.

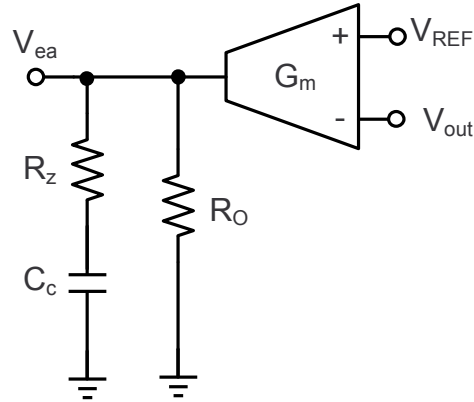


Figure 5.17: A typical compensation implementation of $H(s)$ for current mode control.

The transfer function of this compensator is given by:

$$H(s) = \frac{V_{ea}(s)}{V_{out}(s)} = -G_m R_o \cdot \frac{\frac{s}{\omega_{z1}} + 1}{\frac{s}{\omega_{p1}} + 1} \quad (5.36)$$

where

$$\omega_{z1} = \frac{1}{R_z C_c}, \quad \omega_{p1} = \frac{1}{(R_z + R_o) C_c}$$

R_o represents the output resistance of the operational transconductance amplifier. This transfer function has one low-frequency pole (ω_{p1}) and one zero (ω_{z1}). Typically, ω_{p1} defines the dominant pole of the loop and ω_{z1} cancels or minimizes the effect of the output filter pole ($1/R_L C$).

One drawback of peak current mode control is that when $D > 0.5$, the converter suffers from subharmonic oscillation [3]. This effect is explained in [3], and it can be solved by adding a compensating slope. This compensation slope complicates the design and increases the quiescent power consumption. Another disadvantage is the noise sensitivity, particularly if the inductor ripple current is small [56].

5.6.2.2 Current Sensing Techniques

In this section, several current sensing techniques are presented. Current sensing techniques can be used to measure the inductor current for current mode control or over-current protection [57].

5.6.2.3 Series Sense Resistor

The series sense current sensing method is shown in Figure 5.18. If the value of R_s is known, the inductor current can be measured by sensing the voltage across the resistor (V_s). The accuracy of R_s determines the accuracy of this method. An excessively small value of R_s could be comparable to parasitic board/package resistances, thereby reducing measurement accuracy. Moreover, V_s needs to be large enough to

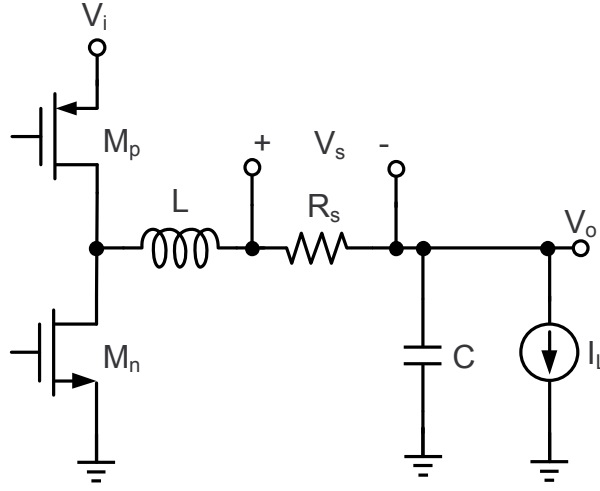


Figure 5.18: Series sense resistor.

overcome the input referred offset of the sense amplifier for practical reasons [57]. Nevertheless, a very large value of R_s would degrade the efficiency of the system since it has the same effect as the DCR of the inductor. This method is undesirable in low-voltage high-current applications where conduction losses are critical.

5.6.2.4 Filter Sense Inductor

In this technique, an RC filter is placed in parallel with the inductor as shown in Figure 5.19. The voltage across the inductor (V_L) is given by:

$$V_L = V_{SW} - V_o = I_L \cdot (L \cdot s + DCR) = I_L \cdot DCR \cdot \left(\frac{L}{DCR} s + 1 \right) \quad (5.37)$$

From Figure 5.19, the voltage across capacitor C_c is then given by:

$$V_c = \frac{V_L}{1 + sR_cC_c} = I_L \cdot DCR \cdot \left(\frac{\frac{L}{DCR}s + 1}{1 + sR_cC_c} \right) \quad (5.38)$$

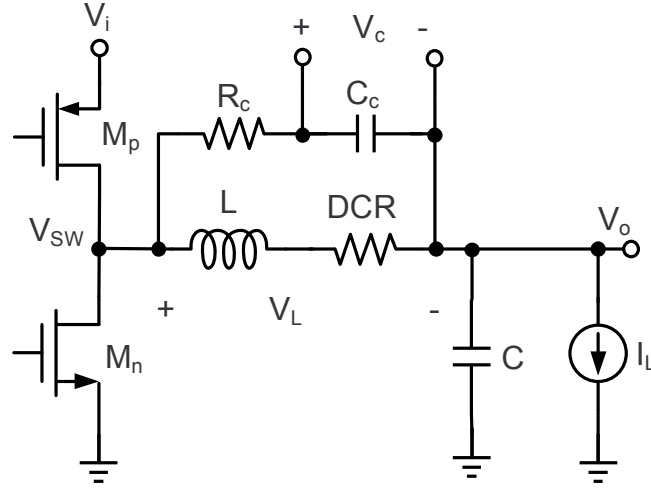


Figure 5.19: Filter sense the inductor.

If the pole $1/(R_c C_c)$ is placed at the same frequency of the zero (DCR/L) , then V_c is proportional to I_L :

$$V_c = I_L \cdot DCR \quad (5.39)$$

This technique is popular because it is relatively lossless when compared with the sense series resistor technique and has good accuracy [47]. A drawback of this technique is that the values of DCR and L need to be known, to select the values of R_c and C_c properly. In addition, it is difficult to have an integrated version of this technique due to the size of R_c and C_c and the required tolerance of the components [57].

5.6.2.5 Sense Fets

Figure 5.20 shows the sense FET current sensing technique. In this technique, a current sensing transistor M_s is placed in parallel with the power transistor M_p . Notice that both transistors share the gate and source, and the effective width of M_s is K times smaller than M_p . Hence, I_s is a scaled version of I_p . K is usually

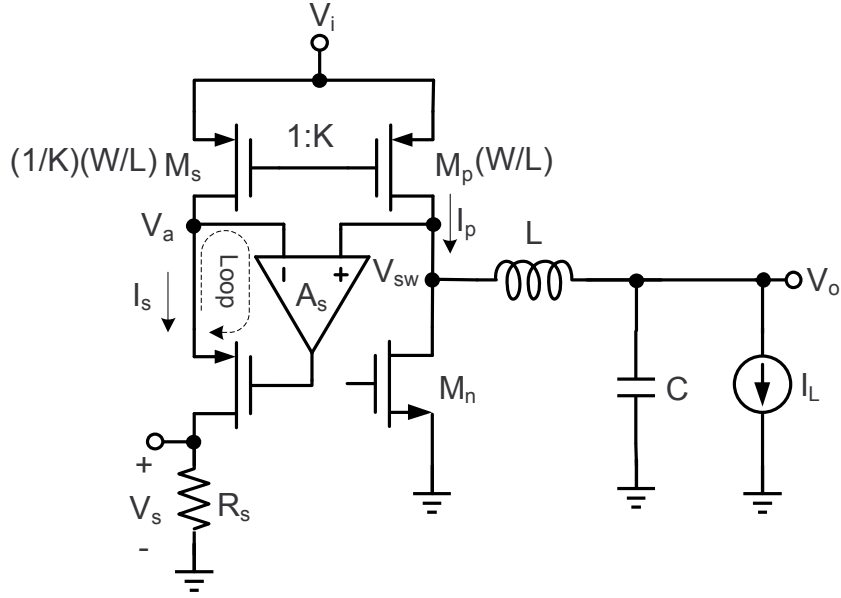


Figure 5.20: Sense Fet method.

larger than 100 to minimize the quiescent power consumption for large I_p . Amplifier A_s is added to make $V_{sw} = V_a$ to minimize channel length modulation and improve current mirror accuracy. The stability of the loop needs to be guaranteed for this technique to operate properly. Moreover, the loop bandwidth should be large enough to include the high frequency components of I_p . Hence, voltage V_s is proportional to I_p :

$$V_s = I_s \cdot R_s = \left(\frac{I_p}{K} \right) \cdot R_s \quad (5.40)$$

This particular implementation only contains the positive slope information of the inductor current and hence, it is useful for peak current mode control and over-current protection. If both slopes of the inductor current are required, another sense transistor can be added in parallel with M_n to obtain the negative slope of the inductor current [51], [58]. This technique is appropriate for an integrated implementation.

5.6.3 Hysteretic Compensation

Hysteretic compensation is also known as bang-bang control [59]. A block diagram of a buck converter with hysteretic voltage mode control is illustrated in Figure 5.21. Notice that this topology is very simple, and its implementation does

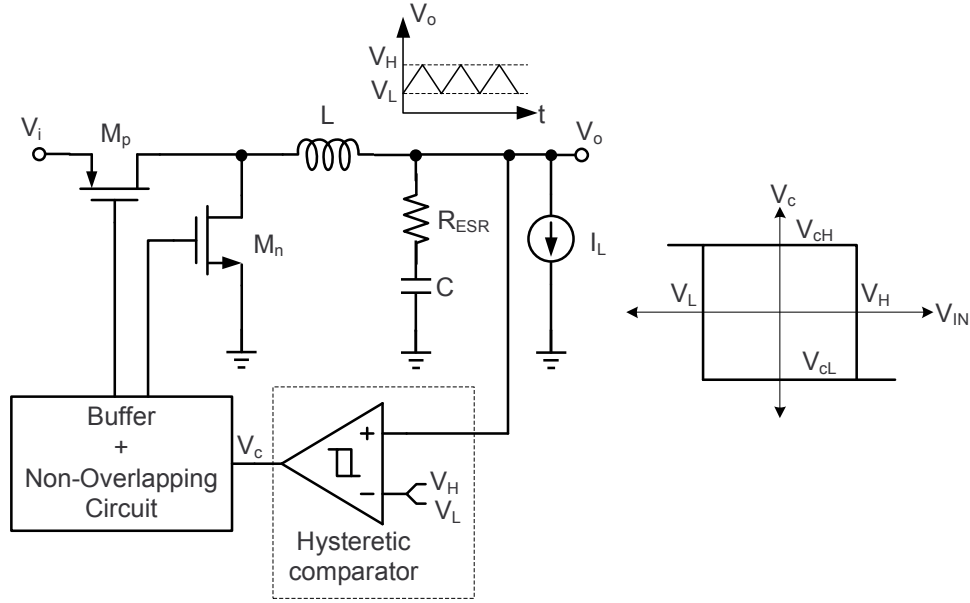


Figure 5.21: Block diagram of a buck converter with hysteretic compensation.

not require resistors or capacitors for compensation. Moreover, this topology does not use the amplifier and carrier signal generator utilized in PWM topologies. This significantly reduces the quiescent power and as a result, this architecture can achieve high efficiency at light loads [59]. In addition, this compensation scheme can react to load transient events in the same cycle that they occur [60]. One drawback of this compensation is that f_s is variable. This variation in f_s makes electromagnetic interference (EMI) shielding in electronics equipment difficult [61]. The operation of

this system can be described as follows: if $V_o > V_H$, then V_o is discharged by turning off M_p and turning on M_n . If $V_o < V_L$, then V_o is charged by turning on M_p and turning off M_n . Hence, V_o is always between V_H and V_L , and the average value of V_o is $V_L + (V_H - V_L)/2$. Assuming that output voltage ripple (Δv_o) is only due to R_{ESR} ,

$$\Delta v_o = V_H - V_L = R_{ESR} \cdot \Delta i_L \quad (5.41)$$

where

$$\Delta i_L = \frac{(V_i - V_o) V_o}{V_i L f_s} \quad (5.42)$$

From (5.41) and (5.42), f_s is found to be:

$$f_s = \frac{V_o (V_i - V_o) R_{ESR}}{V_i L (V_H - V_L)} \quad (5.43)$$

where $(V_H - V_L)$ is the hysteresis window of the comparator. As can be observed the switching frequency depends on the output filter components, input and output voltage, and hysteresis window. Also, notice that the switching frequency is proportional to R_{ESR} . This could be an issue since typically capacitors with small R_{ESR} are required for load transient purposes but this makes f_s very low. Equation 5.43 does not include the effects of the C, equivalent series inductance (ESL), or the delay due to the comparator and drivers on the output voltage ripple. These effects complicate f_s estimation and control [62]. A modified hysteretic controller has been proposed in [60] to minimize the dependency of f_s on the output capacitor and its parasitics (R_{ESR} , ESL). Nevertheless, this technique increases the cost of the system since it requires two additional capacitors and a resistor. A possible implementation of the hysteretic comparator is shown in Figure 5.22 [59]. Signal Q is used to control the power transistors. If $V_{IN} > V_H$, then $S_{bar} = 0$, $R_{bar} = 1$, and $Q = 1$. If $V_L < V_{IN} <$

V_H , then $S_{bar} = 1$, $R_{bar} = 1$, and $Q = Q_{prev}$. Finally, if $V_{IN} < V_L$, $S_{bar} = 1$, $R_{bar} = 0$, and $Q = 0$.

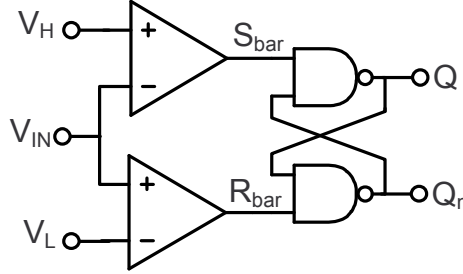


Figure 5.22: Hysteretic comparator.

5.6.4 Sliding Mode Control Compensation

Sliding mode control (SMC) was first proposed in the 1950's in the Soviet Union. SMC is mostly used in systems with variable structures. Switching converters are examples of systems with variable structures because during each subinterval of operation, the differential equations describing the system change. Sliding mode control provides rejection to external perturbations, robustness to parameter variations, and relatively simple implementations [63]–[66]. Figure 5.23 depicts the block diagram of a buck converter implemented with sliding mode control.

The converter is a tracking system that minimizes the voltage error ($V_e = V_{REF} - V_{OUT}$) with the sliding mode controller. Notice that this topology does not require the carrier signal generator utilized in PWM topologies and as a result, area and quiescent power consumption are reduced.

The design of the sliding mode controller is based on the state variables of the desired system to be controlled. In the case of the buck converter, the low-pass

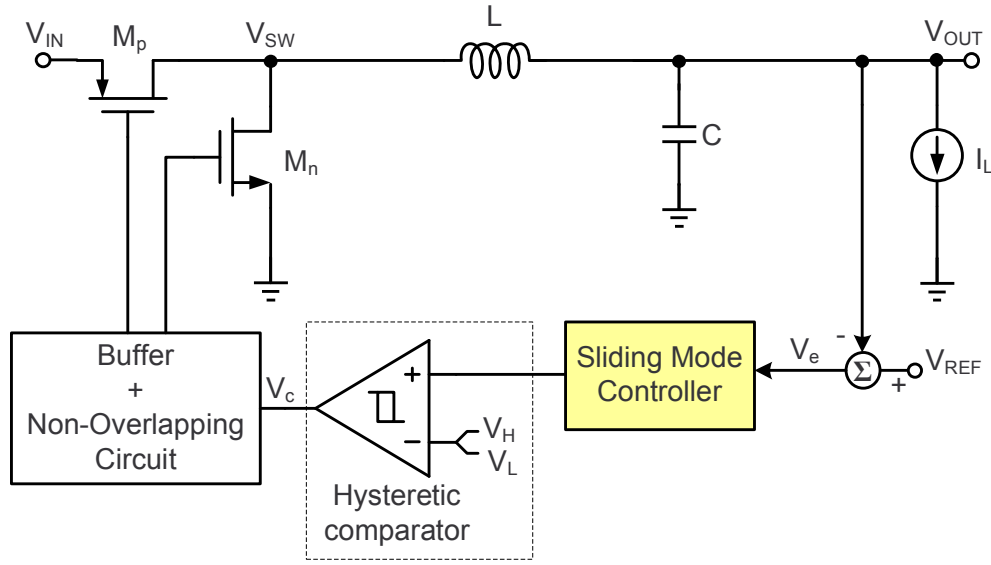


Figure 5.23: Block diagram of a buck converter implemented with sliding mode control.

filter and the power switches are used for the analysis. In Figure 5.24, two different structures can be observed during one cycle of operation.

During the first subinterval (Figure 5.24 (a)), M_p is closed and M_n is open, hence $V_{SW} = V_{IN}$. During subinterval II (Figure 5.24 (b)), M_p is open and M_n is closed, thus $V_{SW} = \text{GND}$. The SMC generates a control function, i.e., control law/switching function (SF), to stabilize the system. The control function makes the system switch between its different structures until the system reaches its sliding equilibrium point (SEP) [64]-[66]. The buck converter is designed to have an SEP is given by:

$$SEP = (V_{REF}, I_{OUT}) \quad (5.44)$$

For example, Figure 5.25 shows the phase portraits for both structures when $V_{REF} = 0.9 \text{ V}$ and $I_{OUT} = 50 \text{ mA}$. The phase portrait in Figure 5.25 (a) corresponds to

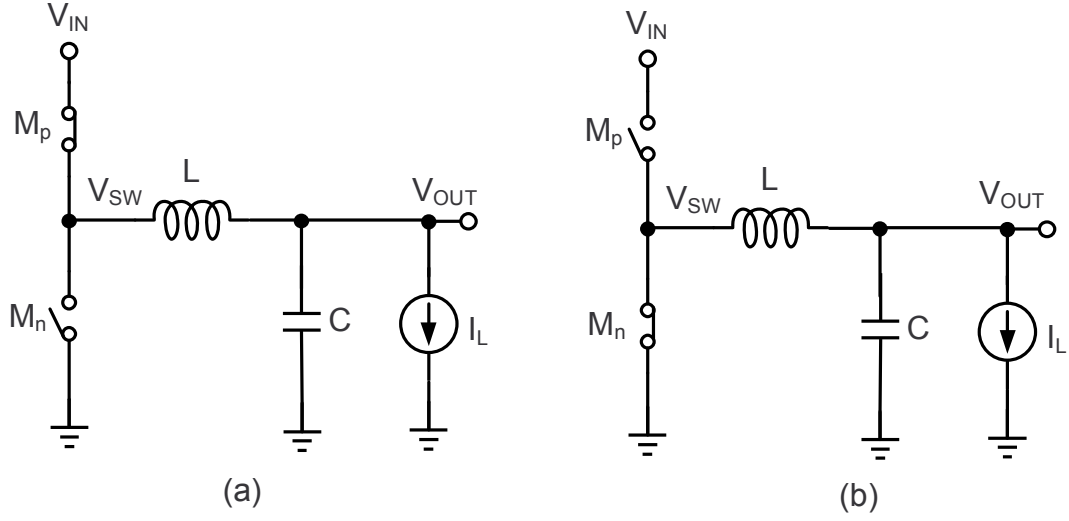


Figure 5.24: Subintervals in a buck converter (a) subinterval I (b) subinterval II.

structure I in Figure 5.24(a). This portrait represents the trajectories of the dynamic system modeled when $V_{SW} = V_{IN}$. Each trajectory represents the motion of the state space variables v_{C2} and i_{L2} in the phase plane. Even though structure I converges to a stable focus equilibrium point [64]-[66], it does not converge to the desired SEP (0.9 V, 50 mA). Similarly, the phase portrait in Fig. 5.25 (b) corresponds to structure II, in Figure 5.24 (b), when the $V_{SW} = \text{GND}$. As in the previous case, structure II does not converge to the SEP. Therefore, a controller is necessary because the SEP is never reached. By designing an appropriate SMC, the SF will make the system to toggle between both structures, creating a sliding surface. In other words, regardless of the initial conditions, the dynamics of the system would move toward the sliding surface until they hit it. Once there, the system will slide in direction of the equilibrium point. Figure 5.26 illustrates the phenomenon.

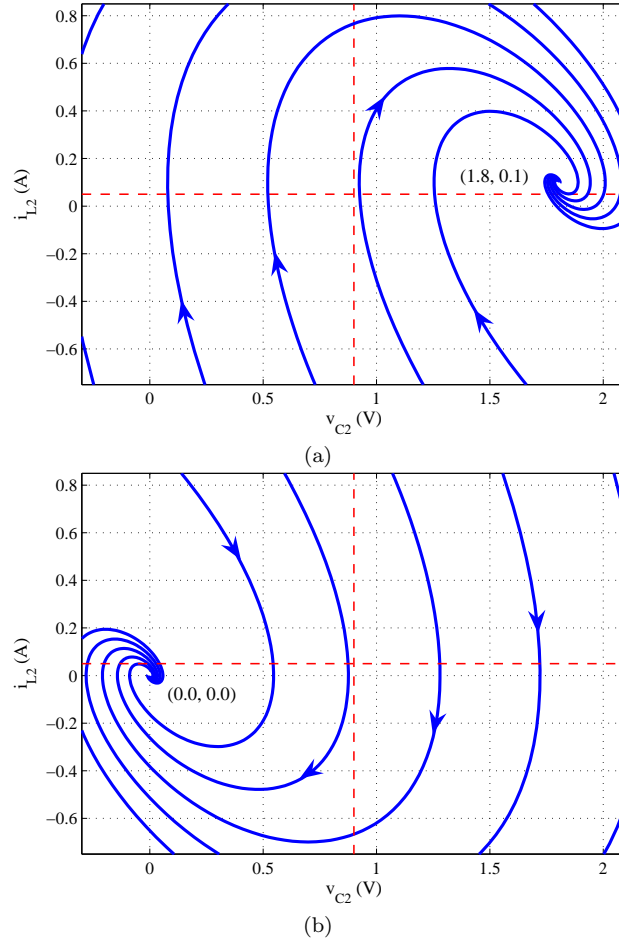


Figure 5.25: Phase portraits of V_{OUT} (a) phase portrait of structure I and (b) phase portrait of structure II.

The SF of the sliding mode controller is defined as:

$$S(V_e, s) = (1 + \alpha s)V_e(s) \quad (5.45)$$

where α is calculated to meet the Hurwitz stability criterion and to guarantee a smooth and fast transient response [64]-[66].

In general, for a k^{th} -order system, sliding mode theory requires a $(k - 1)^{th}$ -order controller [63]-[66]. Since the buck converter is modelled as a second-order system,

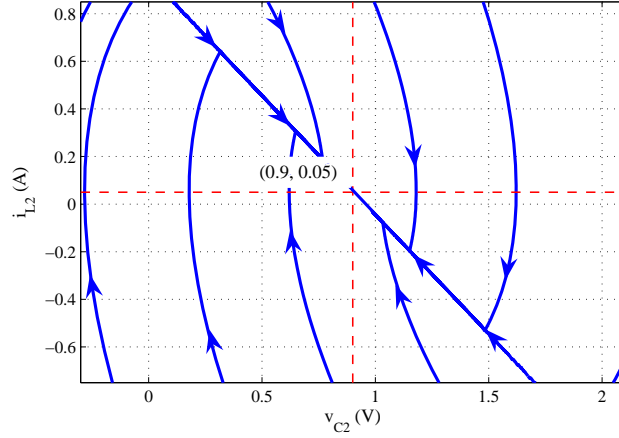


Figure 5.26: Phase portrait of the controlled system trajectories of V_{OUT} under sliding-mode operation.

the controller dynamics are defined by a first-order equation. The switching function is defined as the sum of V_e and its derivative multiplied by a constant. The system can be proved to be asymptotically stable [63]–[66] since the sliding equilibrium point is a stable node with an eigenvalue that is real and negative. The SMC would make each subsystem switch according to the sign of the SF as:

$$V_{SW} = \begin{cases} V_{IN} & \text{when } s(V_e, t) > 0 \\ 0 & \text{when } s(V_e, t) < 0 \end{cases} \quad (5.46)$$

5.6.5 Digital Control Compensation

Digital PWM control has several advantages over analog control such as: robustness to parameter variations, programmability, and reduction or elimination of external passive components for compensation, and calibration [67]. Figure 5.27 shows a block diagram of a buck converter with digital PWM control. As can be seen from Figure 5.27, digital PWM control consists of an analog to digital converter (ADC), a digital filter (compensator), and a digital PWM (DPWM). This circuit

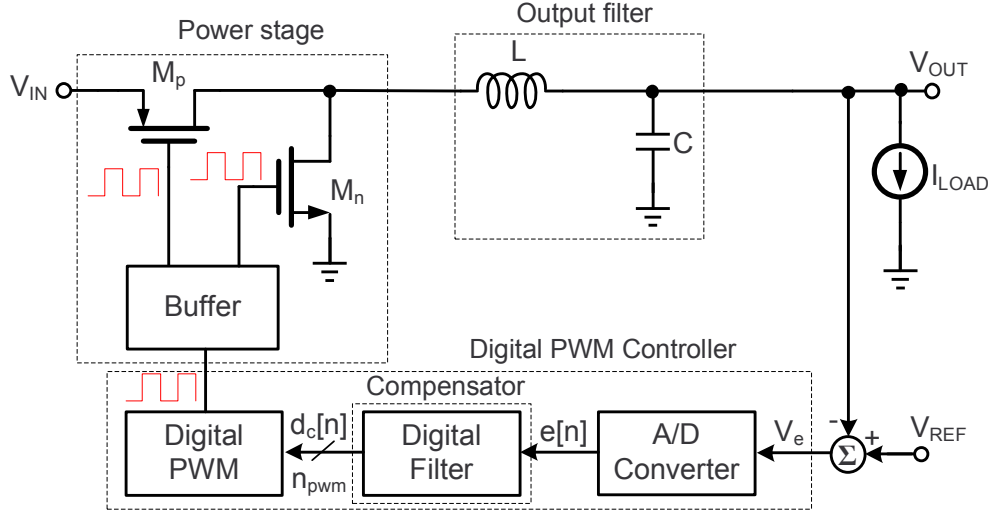


Figure 5.27: Block diagram of a buck converter with digital control.

operates as follows: The voltage error, $V_e = V_{REF} - V_{OUT}$, is sampled and converted to a digital error signal $e[n]$ by the ADC. Then, the digital filter calculates the digital duty-cycle $d_c[n]$ command, and the DPWM generates a signal with the desired f_s and duty cycle to control the power stage.

There are some challenges in the implementation of a digital PWM control; for example, the ADC conversion time should be in the order of 100 ns for switching frequencies in the MHz range [67]. In addition, an ADC with a resolution of 6 bits or more is typically required to achieve good voltage regulation. An ADC with this kind of performance could consume more power and chip area than the entire analog controller. Delay-line based windowed ADC has been proposed to tackle the power consumption issue [68]. The resolution of the DPWM must be higher than the one of the ADC to avoid limit-cycle oscillations and as a result, high power consumption is typically required in the DPWM. A survey of possible DPWM implementations for digital control of switching DC-DC converters is offered in [69]. In general, a buck

converter implemented with digital PWM control consumes higher power than one implemented with analog control [70].

5.6.6 Compensation Scheme Summary

Table 5.2 summarizes the advantages and disadvantages of each compensation scheme presented in this section.

Table 5.2: Summary of advantages and disadvantages of the different compensation schemes

Compensation scheme	Advantages	Disadvantages
Voltage Mode PWM (Type-III)	Constant f_s , predictable EMI, good load transient response, predictable performance	Area by compensation components, Complicated compensation
Current Mode PWM (Peak)	Inherent current protection, good transient, first-order system, simpler compensation constant f_s	Sub-harmonic oscillation for $D > 0.5$, Noise sensitivity for small inductor current ripple and light loads, complexity
Hysteretic	Fast transient response, no passive compensation components, small quiescent power	Variable f_s , Unpredictable EMI,
Sliding Mode	Fast transient response, few passive compensation components, small quiescent power	Variable f_s , Unpredictable EMI
Digital	Robustness to parameter variation, programmability, reduction or elimination of external passive components, calibration	Quiescent power consumption, area

5.7 Multiphase Interleaved Buck Converter

Figures 5.28 shows the block diagram of a multiphase interleaved buck converter [71]. A multiphase buck converter combines N number of individual buck converters with phase shift in parallel with common input and output connections.

The main advantage of multiphase buck converters is the output current ripple reduction which consequently decreases the output voltage ripple. This allows the use of smaller inductance to improve load transient performance [72] since smaller inductors provide a higher output current slew rate ($di/dt = V_L/L$), where V_L is the inductor voltage. It also reduces the value of the required output capacitance [72]-[73]. In this topology, every stage is operating at f_s but the drivers are synchronized

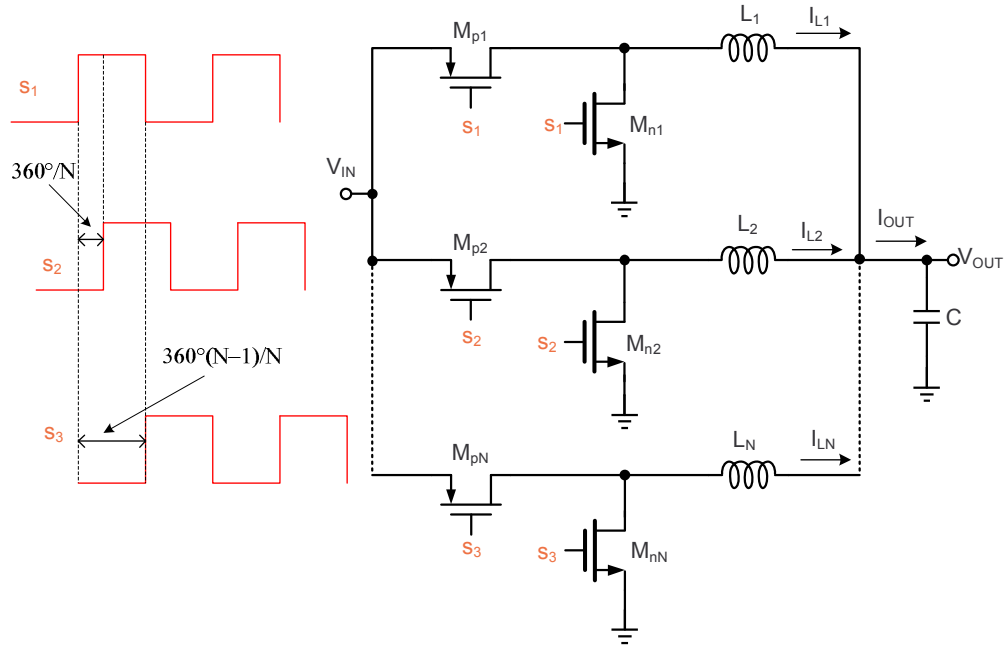


Figure 5.28: Multiphase interleaved buck converter.

such that adjacent phases are shifted by $360^\circ/N$ as shown in Figure 5.28. The output current ripple in a multiphase interleaved buck converter is given by [72]:

$$\Delta i_L = \left(\frac{V_{OUT} \cdot (1 - D)}{L \cdot f_s} \right) \cdot \left(\frac{N \cdot \left(D - \frac{m}{N} \right) \cdot \left(\frac{m+1}{N} - D \right)}{D \cdot (1 - D)} \right) \quad (5.47)$$

where N and m are the number of phases in the buck converter, and the maximum integer that does not exceed product $N \cdot D$, respectively.

Figure 5.29 shows the output current ripple versus duty cycle for different N values.

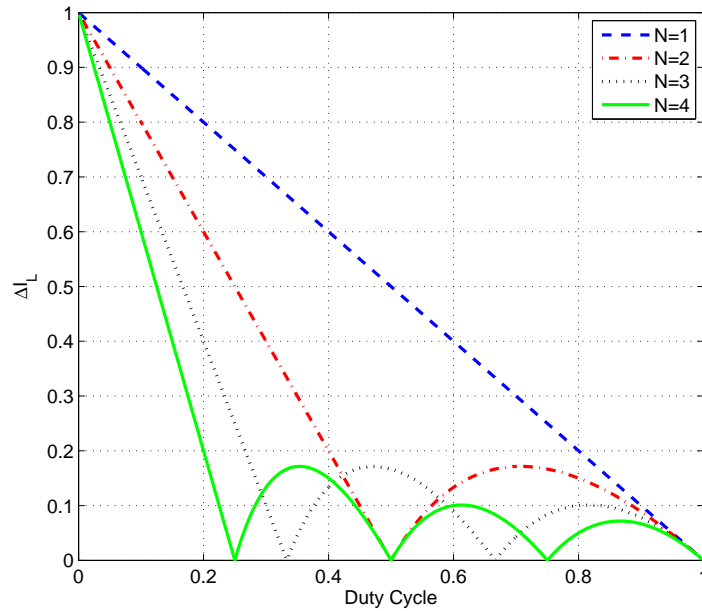


Figure 5.29: Output current ripple versus duty cycle for different N values.

Notice that if D is a multiple of $1/N$, complete output current ripple cancellation can be achieved. For the same I_{OUT} , the power rating of the power transistors and inductors in an N -phase converter can be reduced by N when compared with a one-phase converter.

5.8 Practical Design Considerations for Switching Converters

In this section, key design considerations for buck converters in practical implementations, such as building blocks design and integrated circuit layout techniques, are presented. In addition, some printed circuit board (PCB) design and layout techniques are provided.

5.8.1 Building Blocks

5.8.1.1 Comparator

Figure 5.30 shows the transistor level implementation of a popular hysteretic comparator in the literature [74]. The first stage (M_1 - M_3) has a source-coupled differential pair with positive feedback to achieve high gain. The gain of this stage is given by [75]:

$$A_{v1} = \sqrt{\frac{\mu_p(W/L)_1}{\mu_n(W/L)_3}} \cdot \frac{1}{1 - \alpha} \quad (5.48)$$

where $\alpha = (W/L)_2/(W/L)_3$. The hysteresis window of this comparator can be expressed as [75]:

$$V_{hys} = 2\sqrt{\frac{I_{M6}}{K_p}} \left(\frac{1 - \sqrt{\alpha}}{\sqrt{1 + \alpha}} \right) \quad (5.49)$$

For (5.49) to be valid, parameter α must be greater than 1. The second-stage(M_4 - M_5) provides additional gain ($2g_{m4}/(g_{ds4} + g_{ds5})$) and class-AB driving capability. The inverter chain (M_7 - M_{10}) is used to achieve rail-to-rail output swing.

The comparator must also achieve minimum propagation delay and low input offset. A propagation delay in the order of several ns for switching frequencies below 1 MHz is acceptable [74]. In addition, the comparator input common mode range must match the output common mode range of the compensator. Another common comparator utilized in buck converters is shown in Figure 5.31.

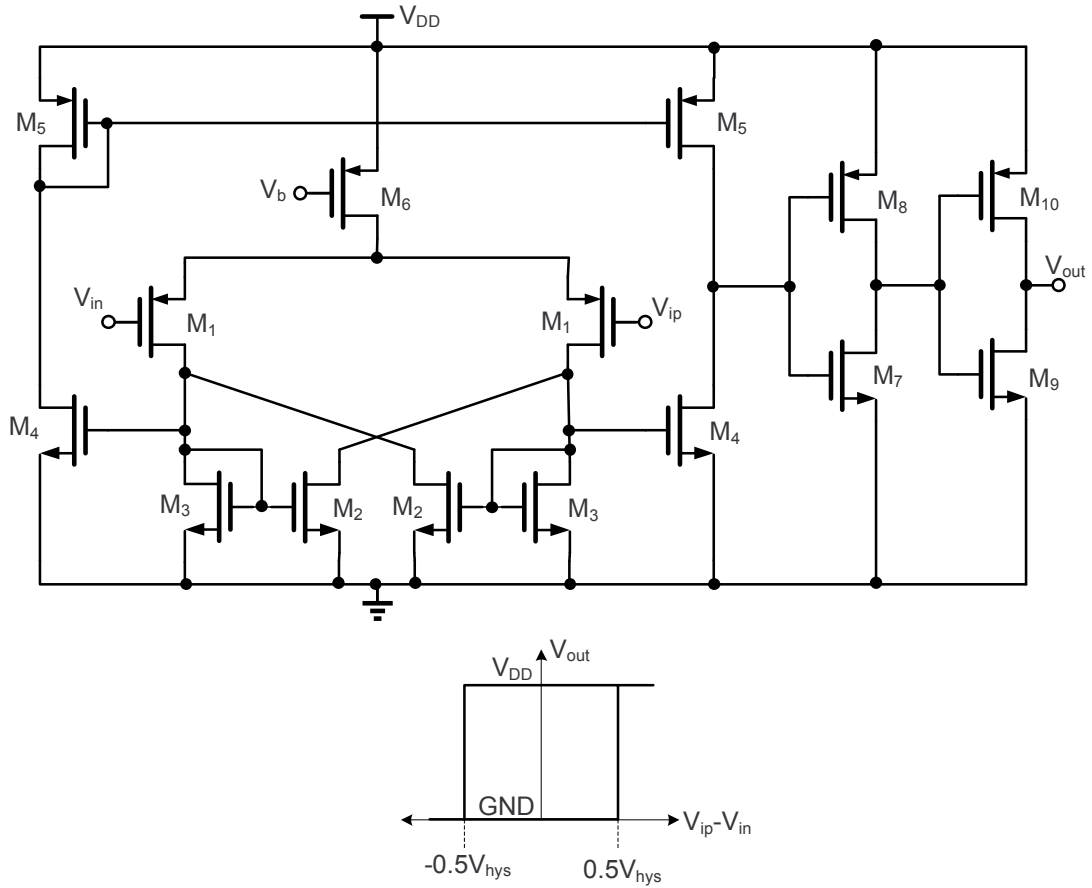


Figure 5.30: Transistor level of the comparator.

Notice that this comparator consists of a two-stage amplifier (M_1 - M_5) without compensation and an inverter chain (M_6 - M_9) as output stage to provide rail-to-rail output swing. More details about this comparator can be found in [76].

5.8.1.2 Carrier Signal Generator

Figure 5.32 shows an implementation of a carrier signal generator [77]. During time t_1 , switch S_{ch} is closed (S_{dis} is open), and current I_{ch} charges capacitor C until V_c reaches V_H . After that, switches S_{ch} and S_{dis} are opened and closed, respectively, by the comparison circuit. Then, during time t_2 , I_{dis} discharges capacitor C until

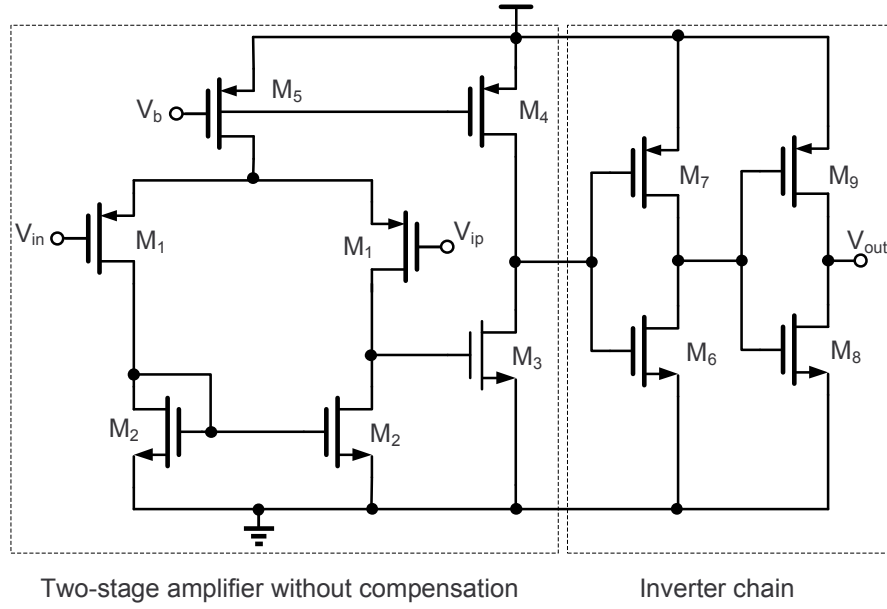


Figure 5.31: A common comparator in buck converter without hysteresis.

V_c reaches V_L and the cycle repeats again. The switching frequency of this circuit is given by:

$$f_s = \frac{1}{t_s} = \frac{1}{t_1 + t_2} \quad (5.50)$$

where

$$t_1 = \frac{C \cdot (V_H - V_L)}{I_{ch}}, \quad t_2 = \frac{C \cdot (V_H - V_L)}{I_{dis}}$$

hence,

$$f_s = \frac{1}{C \cdot (V_H - V_L) \cdot \left(\frac{1}{I_{ch}} + \frac{1}{I_{dis}} \right)} \quad (5.51)$$

If $I_{ch} = I_{dis}$, V_c is triangle wave. If $I_{ch} \gg I_{dis}$ or $I_{ch} \ll I_{dis}$, V_c is a sawtooth wave.

It is important to minimize the delay of the comparators to reduce the error [77].

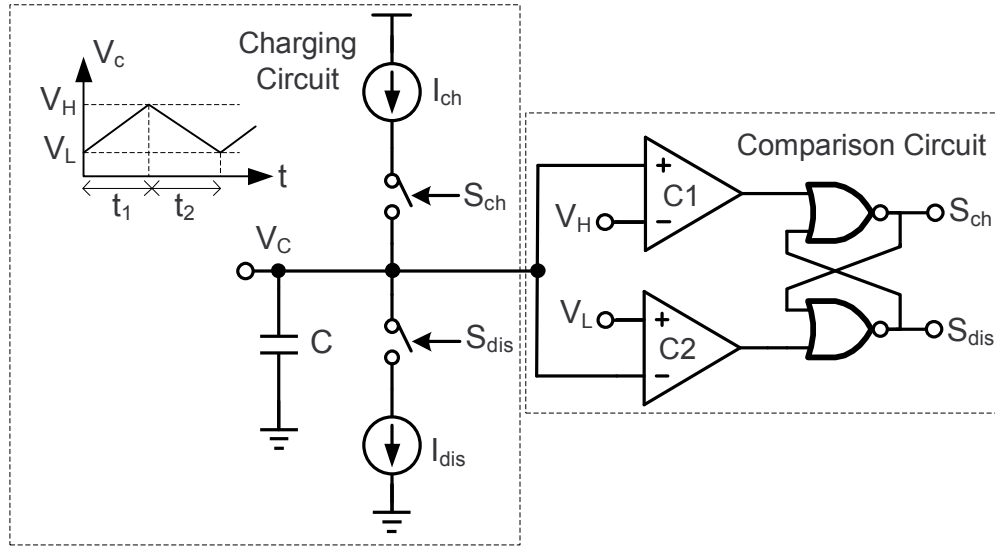


Figure 5.32: Carrier signal generator circuit.

5.8.1.3 Non-Overlapping Circuit

As mentioned previously in this section, a non-overlapping circuit is used to keep both power transistors from simultaneously conducting. Figure 5.33 (a) shows the non-overlapping signals. Signals ϕ_p and ϕ_n control the gates of the PMOS and NMOS power transistors, respectively. Time t_{no} represents the non-overlapping time. Notice that the PMOS transistor turns off (ϕ_p goes high) before the NMOS transistor turns on (ϕ_n goes high), and that the NMOS turns off (ϕ_n goes low) before the PMOS transistor goes turns on (ϕ_p goes low). Figure 5.33 (b) shows a non-overlapping circuit that can generate the signals in Figure 5.33 (a). The delay block determines t_{no} , and it can be implemented with an inverter chain [78].

5.8.1.4 Buffer and Power Transistors

Power transistors are designed to minimize conduction losses. This is achieved by sizing them to reduce their on-resistance (R_{on}). Assuming very small drain to

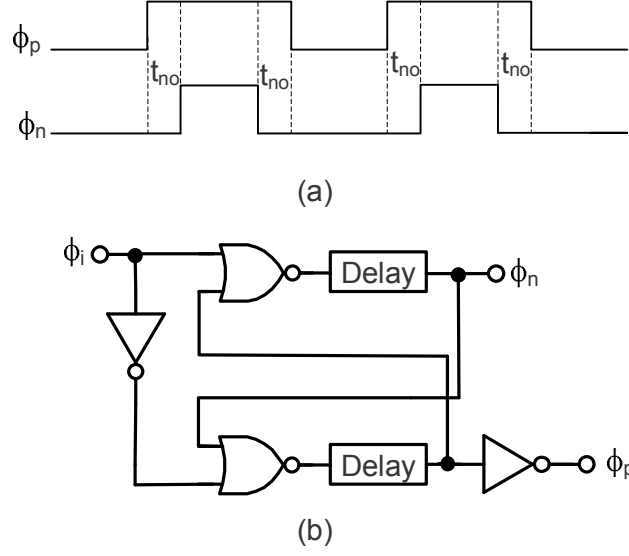


Figure 5.33: Non-overlapping circuit.

source voltage, the R_{on} of a MOSFET is given by:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad (5.52)$$

where μ and C_{ox} are the mobility and gate oxide capacitance per unit area of the transistor, respectively; and V_{TH} is the threshold voltage. Notice that R_{on} is inversely proportional to (W/L) ; hence to minimize R_{on} , a large (W/L) is usually required. The larger the maximum load current, the smaller the desired R_{on} to minimize conduction losses as shown in (5.8).

Buffers are necessary to drive the power transistor (M_p and M_n) and should be optimized to minimize the gate drive power losses (P_{gdrv}) to improve the efficiency at light loads without significantly degrading the propagation delay [59]. For the smallest propagation delay, the optimized scale factor between stages mathematically equals to Euler's number [79]; however, it requires an impractical number of stages

which increases area and switching power consumption. In the next section, an example of how to design the buffers will be provided.

5.8.1.5 *General Layout Recommendations*

Attention needs to be taken with the power stage layout since it determines the efficiency performance of the buck converter. As in the case of LDO voltage regulators, the track resistance (resistance between drain/source and bondpad), bond-wire resistance (resistance between bondpad and pin), and printed board circuit trace resistance—all affect efficiency. To minimize the track resistance, use as many contacts and wide tracks for the drain and source terminals as needed to reduce sheet and via resistances. Top metals should be used for power routing because they have the smallest resistance. Moreover, multiple metals in parallel can also be used to minimize the track resistance. Large diameter bondwires or multiple bond-wires in parallel can be used for the drain and source terminals to reduce bond-wire resistance [20].

As mentioned before, a sense transistor can be placed in parallel with the power transistor for current sensing purposes such as current mode control and over-current protection. The sense and power transistors should be as close as possible to minimize mismatch due to large thermal gradients [20].

Substrate noise generated by the power stage can degrade the analog section performance. To minimize this effect, the analog section should be placed as far as possible from the power stage. In addition, a high resistivity P^- region covered by a shallow trench guard ring can be used to reduce the substrate noise coupling from the power stage to the analog section [80]. This guard ring should be as wide as possible.

Placing as many substrate contacts as possible in the local cells provides homo-

geneous bulk voltage for the transistors. In addition, guard rings should be used to prevent latchup and block noise coupling that may degrade performance [20].

5.8.2 Printed Circuit Board

5.8.2.1 Design

Using ceramic capacitors with low ESR at the output minimizes voltage dip/surge amplitudes ($I_L R_{ESR}$) during load transient events and output voltage ripple. Multiple capacitors can be used in parallel to increase the capacitance and reduce R_{ESR} to improve the load transient response even further and minimize the output voltage ripple. Nevertheless, be aware that ceramic capacitors have a capacitance that is both bias voltage and temperature dependent [81]. Usually, the larger the footprint (size) of the capacitor (E.g. 1210, 1805), the smaller the capacitance variation due to bias voltage. The designer should carefully read the datasheet of the capacitor to verify the capacitance variation due to bias voltage and temperature.

Input capacitors are required to reduce the input voltage ripple and minimize the input voltage deviation during load transients [82]. Ceramic capacitors with small ESR should be placed as close as possible to the input pin to be effective because even a small amount of inductance can increase the input voltage ripples and spikes [82].

5.8.2.2 Layout

The trace resistance at 25° C is given by:

$$R_{trace} = \rho \cdot \frac{L}{W \cdot t} \quad (5.53)$$

where ρ is the resistivity of the material (i.e. $1.7 \cdot 10^{-6}$ Ω -cm for copper). Parameters L, W, and t represent the length, width, and thickness of the trace. Hence, using short and wide traces for power routing lines (i.e. V_{IN} and V_{OUT}) to minimize trace

resistance and power losses is recommended. Also, connecting the feedback trace (connection from V_{OUT} to feedback resistors) as close as possible to the load improves load regulation since the voltage drop through the trace is compensated by the feedback loop. The feedback connections should be routed as far as possible from the switching node V_{SW} to avoid noise coupling to the controller. These recommendations are depicted in Figure 5.34.

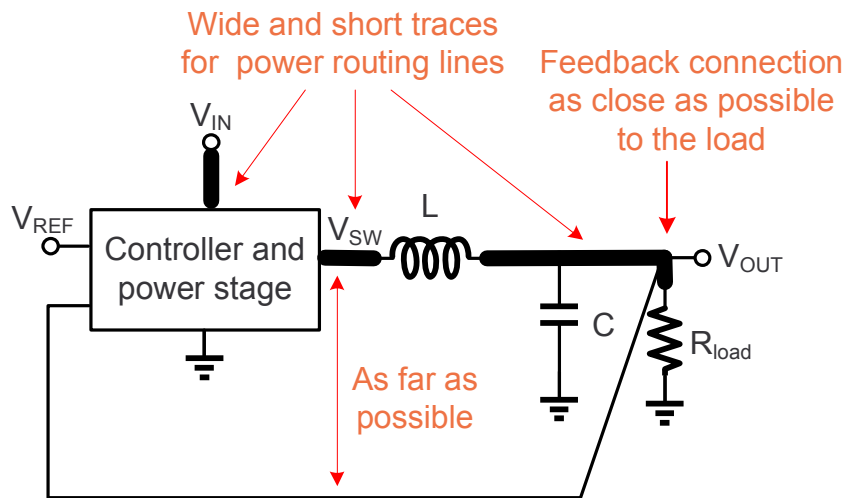


Figure 5.34: PCB design recommendations.

5.9 Measurements

DC-DC switching converter specifications include efficiency, output voltage ripple, current ripple, switching frequency, line/load regulation, and line/load transient.

Basic voltage regulator characterization requires the following measurement equipment: power supplies, multi-meters, an oscilloscope, waveform generators, power resistors, power transistors, and an evaluation board.

5.9.1 Efficiency Measurement Setup

Figure 5.35 shows an efficiency measurement setup. The power efficiency of a DC-DC switching converter is given by:

$$\eta(\%) = \frac{P_{OUT}}{P_{IN}} = \left(\frac{I_L V_{OUT}}{I_{IN} V_{IN}} \right) \cdot 100 \quad (5.54)$$

From (5.54), the efficiency can be calculated by measuring I_L , V_{OUT} , I_{IN} , and V_{IN} with a multi-meter. Currents I_{IN} and I_L can be obtained by measuring voltages V_{R_i} and V_{R_L} , respectively. The output voltage ripple and switching frequency can be also measured with this setup by probing V_{OUT} and V_{SW} nodes and using an oscilloscope to observe the signals.

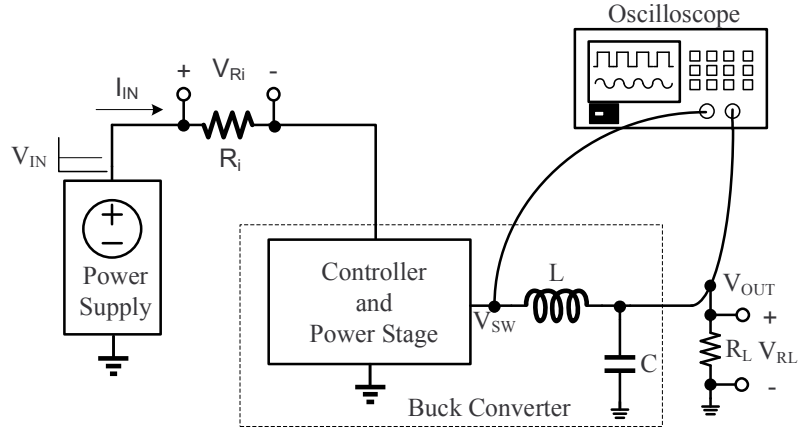


Figure 5.35: Efficiency measurement setup for a buck converter.

5.9.2 Load Transient Measurement Setup

Figure 5.36 shows a load transient measurement setup. The load step is generated by switching the connection between the output voltage V_{OUT} and the load resistance

R_L using the power FET (M_{TEST}). The minimum load current ($I_{L,min}$) is determined by V_{OUT}/R_{LB} and the maximum load current is equivalent to $I_{L,min} + V_s/R_L$. The output voltage and load current step waveforms can be observed in an oscilloscope since I_L is directly proportional to R_L . Load regulation can be obtained if the measurements are performed in steady-state.

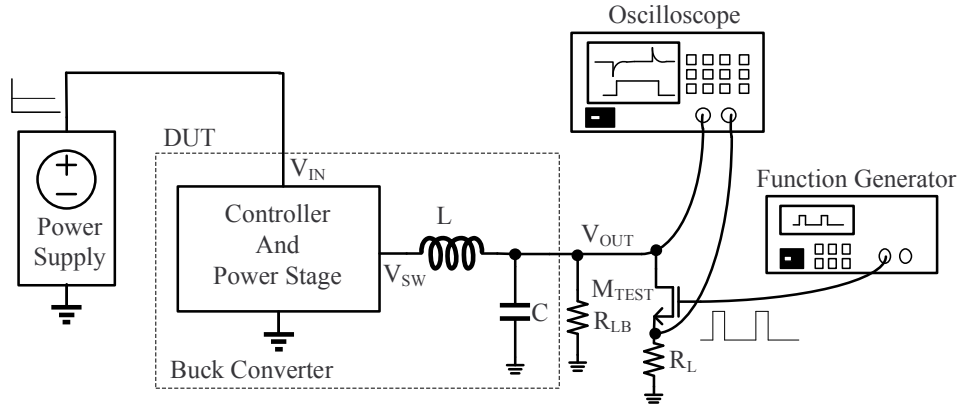


Figure 5.36: Load transient measurement setup for a buck converter.

5.9.3 Line Transient Measurement Setup

Figure 5.37 shows a line transient measurement setup. The line transient test can be performed with an square signal superimposed on a DC voltage level. A driver is added between the waveform generator and the input of the buck converter to provide the required input current. This is particularly necessary at heavy loads since a waveform generator is not capable of providing currents above a few milliamps. This driver must be able to handle the input capacitance of the buck converter. Line regulation can be also obtained if the measurements are performed in steady-state.

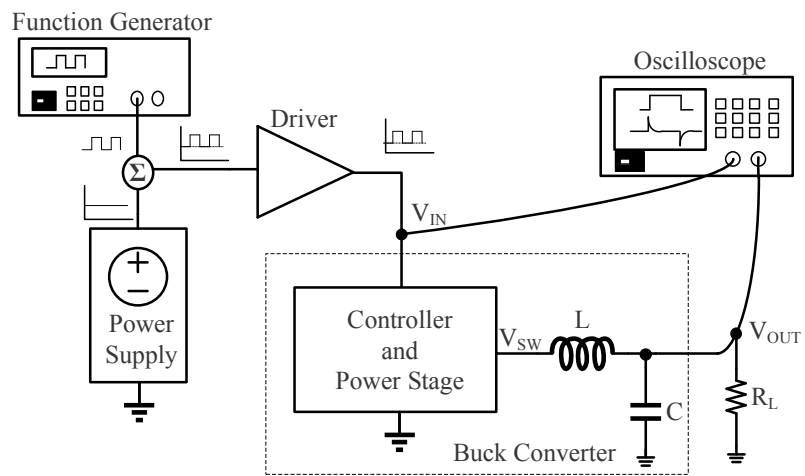


Figure 5.37: Line transient measurement setup for a buck converter.

6. AREA REDUCTION TECHNIQUES FOR BUCK CONVERTERS*

6.1 Introduction

The main advantage of a buck converter over other step down voltage converters is its high efficiency. However, its main drawback is probably the high cost of the off-chip output filter components (e.g., output filter inductor) and the large area occupied when compared with linear voltage regulators and charge pumps. Figure 6.1 shows the block diagram of a conventional converter. The passive components of the

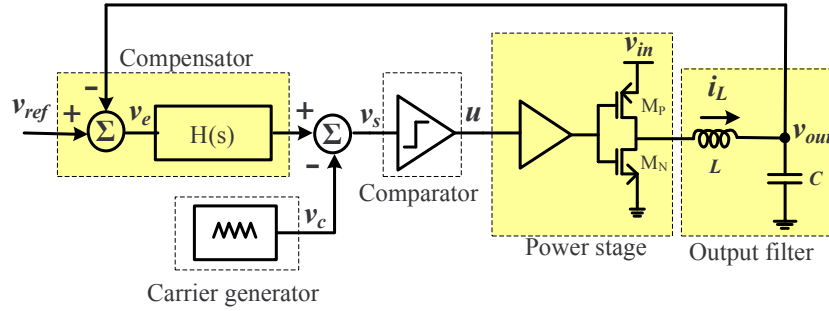


Figure 6.1: Block diagram of the buck converter.

compensator, power stage, and output filter occupy most of the area in a buck

*

* Part of this section is reprinted with permission from “Design of a Fully-Integrated Buck Voltage Regulator Using Standard CMOS Technology” by M. A. Rojas-Gonzalez, J. Torres, and E. Sanchez-Sinencio, *IEEE Third Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 1-4, March 2012, © 2012 by IEEE.

* Part of this section is reprinted with permission from “Design of an integrated single-input dual-output 3-switch buck converter based on sliding mode control” by M. A. Rojas-Gonzalez, J. Torres, and E. Sanchez-Sinencio, *Analog Integrated Circuits and Signal Processing*, vol. 76, no. 3, pp. 307-319, September 2013.

converter. This section introduces several area reduction techniques for the buck converter, which apply to its output filter, output power stage, and compensator.

Firstly, the design of a fully integrated buck converter using a standard 0.18 μm CMOS technology is presented. The converter employs a dual-phase structure to minimize the output voltage ripple. The controller is implemented using a hysteretic architecture based on sliding-mode theory. The external low pass filter has been integrated on-chip by increasing the switching frequency up to 45 MHz.

Secondly, the design and implementation of a single-input dual-output buck converter is presented. The proposed topology implements only three switches instead of the four switches used in the conventional solution, thus potentially reducing area in the power stage through proper design of the power switches.

Thirdly, a compensation scheme that employs a combination of Gm-RC and Active-RC techniques to emulate the conventional voltage mode Type-III compensation is proposed. This compensator reduces area by more than 45 % when compared with the conventional Type-III compensator, while consuming low quiescent power and achieving good line/load regulation. The total active area of the buck converter is decreased by approximately 15%. Finally, conclusions are provided.

6.2 Buck Converter Output Filter Area Reduction

In low power applications, traditional buck converter implementations integrate the compensator, carrier signal generator, comparator, and power stage; however, the output filter is typically implemented with off-chip components due to their large size. Typical switching frequencies are in the order of hundreds of kilohertz to a few megahertz. At such frequencies, the values of the filter inductor and capacitor are in the order of μH and μF , respectively [2]. These values restrict the full integration of the switching converter.

A fully-integrated buck converter would reduce the number of off-chip components and printed circuit board (PCB) area, thereby significantly reducing the total cost of the system. In addition, energy losses can potentially be minimized due to a reduction in the interconnection parasitics between the integrated circuit (IC) and the external components. Hence, it is necessary to reduce the filter inductor and capacitor to the order of nH and nF, respectively. This can be achieved by increasing the switching frequency to the order of tens of megahertz [2]. However, several key drawbacks such as the effect of a low quality factor inductor (large parasitic resistance) and high switching frequency in the efficiency performance need to be addressed. For more details about how these factors affect the buck converter efficiency see section 5.5.

6.2.1 Multi-Phase Interleaved Buck Converter

Integrating LC-filter passive components demands a higher switching frequency to obtain sufficiently small components values. The value of the output filter inductor L and the output filter capacitor C in Figure 6.1, assuming CCM operation [2] are:

$$L = \frac{V_{IN} (1 - D) D}{2 \Delta i_L f_s} \quad (6.1)$$

$$C = \frac{\Delta i_L}{8 \Delta v_C f_s} \quad (6.2)$$

where D , f_s , Δi_L , Δv_C represent the duty cycle, the switching frequency, the inductor current ripple, and the output voltage ripple, respectively.

However, due to dynamic losses proportional to the frequency of operation [2], increasing the switching frequency degrades the switching regulator's efficiency. A possible solution to this drawback is the use of an interleaved synchronous converter operating at lower frequency in parallel configuration, e.g., multi-phase structure [83]-[84].

A multi-phase buck converter is the combination of many individual buck converters sharing the same load. These converters are connected in such way that the current they deliver adds to the output node. Moreover, output ripple can be reduced if the drivers of each stage are synchronized such that adjacent phases are shifted by $360^\circ/N$.

6.2.2 Proposed Dual-Phase Buck Converter Architecture

The proposed architecture is shown in Figure 6.2. The converter implements a

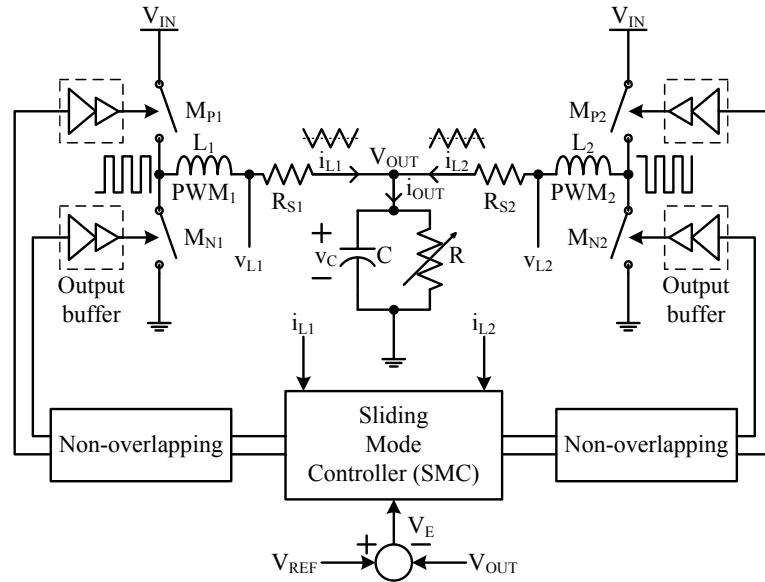


Figure 6.2: Proposed fully-integrated voltage regulator architecture.

two-phase topology ($N = 2$), which can effectively reduce the output current ripple by at least half. If both stages are 180° out-of-phase and the duty cycle is 0.5, complete cancellation of the output current ripple occurs. Mismatch between the paths would prevent full cancellation. The generation of the interleaved pulse-width modulated signals, PWM_1 and PWM_2 , is done by employing a hysteretic controller

based on sliding mode control [85]. For more details about multi-phase interleaved buck converters see section 5.7.

The interleaved output currents (i_{L1} and i_{L2}) are generated by sensing the currents across the respective output inductors and processing them in the controller. The effective switching frequency becomes $2f_s$ and the LPF passive components values can be further reduced by half. More details about the controller can be found on [21], [86].

The dual-phase fully-integrated buck converter regulator has been designed in 0.18 μm CMOS standard technology with an input voltage (V_{IN}) of 1.8 V. The output voltage (V_{OUT}) is 1 V with a maximum output current ($I_{L,max}$) of 400 mA. The switching frequency is 45 MHz and the output current and voltage ripples are $\Delta i_L = 100$ mA and $\Delta v_C = 50$ mV, respectively. The value of the passive components are $L = 24.5$ nH and $C = 2.75$ nF.

6.2.3 Integrated Output Low-Pass Filter

6.2.3.1 Output Capacitor

The output capacitor is built using MOS capacitors, or MOSCAPs, because they provide the highest capacitance per area when compared to metal-to-metal and poly-to-poly implementations [84]. Figure 6.3 shows the implementation of a MOSCAP with an NMOS transistor. The equivalent capacitance of a MOSCAP is given by:

$$C = Area \cdot C_{ox} = W \cdot L \cdot C_{ox} \quad (6.3)$$

where W , L , and C_{ox} are the width, length, and gate capacitance per unit area of the transistor, respectively.

The size of the unit cell MOSCAP is optimized by calculating the minimum equiv-

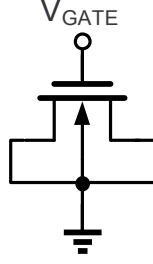


Figure 6.3: MOSCAP implementation.

alent series resistance (ESR) of the capacitor [87]-[88]. The model for the ESR (in Ω) of a MOS capacitor [87], neglecting external resistance and frequency dependence, is

$$ESR = \frac{1}{\mu C_{ox} (V_{gs} - V_T)} \frac{L}{W} + \alpha R_{poly} \frac{W}{L} \quad (6.4)$$

where the first term represents the channel resistance and the second term the polysilicon resistance. Parameters μ , V_{gs} , V_T , and R_{poly} are the mobility, the gate-source voltage, the threshold voltage, and the polysilicon sheet resistance (in Ω/\square), respectively. The factor α equals to 1/12 if the gate is connected from two sides and 1/3 if it is connected from one side.

The minimum equivalent series resistance for a single MOS capacitor can be calculated by differentiating (6.4) with respect to the aspect ratio (W/L) of the transistor. The optimum aspect ratio of the transistor and the minimum ESR are given by:

$$\left(\frac{W}{L}\right)_{opt} = \sqrt{\frac{1}{\alpha \mu C_{ox} (V_{gs} - V_T) R_{poly}}} \quad (6.5)$$

$$ESR_{min} = 2 \sqrt{\frac{\alpha R_{poly}}{\mu C_{ox} (V_{gs} - V_T)}} \quad (6.6)$$

The optimum width and length of the MOSCAP cell is $W_{opt} = 22 \mu\text{m}$ and $L_{opt} =$

800 nm with $ESR_{min} = 36 \Omega$ for $\mu C_{ox} = 314 \mu\text{A}/\text{V}^2$, $R_{poly} = 7.7 \Omega$, and $\alpha = 1/12$. The number of unit cells is 16919 and the total ESR is $ESR_T = ESR_{min}/16919 = 2.1 \text{ m}\Omega$.

6.2.3.2 Output Inductor

The physical dimensions of the output inductor are customized due to the large amount of current that it needs to handle [84], [89]. The characterization of the inductor is optimized using SONNET[†] simulator. The schematic model from software simulation is shown in Figure 6.4. The main drawback of the integrated inductor is

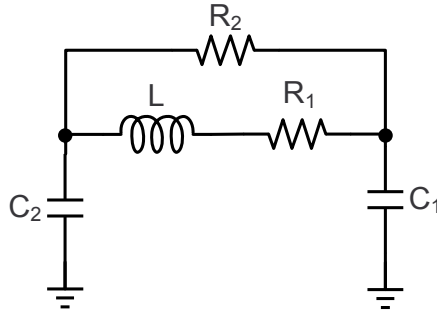


Figure 6.4: Extracted schematic inductor model.

its high equivalent series resistance (R_1) due to the poor conductivity, the high sheet resistance, and the relatively thin ($2.4 \mu\text{m}$) top metal layer. Table 6.1 summarizes the extracted schematic values of the inductor model and estimates the hypothetical sizes of the model with thicker metal layer. Values of parasitic capacitors C_1 and C_2 are 200 fF and 500 fF, respectively. The quality factor of the inductor ($Q_L = \omega L/R_1$) improves if a thicker top metal layer is used. Also, the use of a metal with

[†]<http://www.sonnetsoftware.com/>.

Table 6.1: Component values of the schematic inductor model

Metal thickness	1X	2X	5X	10X
L	24.5 nH	22.8 nH	22.7 nH	23.7 nH
R_1	2.7 Ω	1.6 Ω	0.9 Ω	0.6 Ω
R_2	62 Ω	147 Ω	329 Ω	385 Ω
Q_L	2.85	4.48	7.92	12.41

better conductivity and/or magnetic materials could boost the quality of the output inductor. In [83], high-quality aircore inductors are utilized to minimize conduction power losses, and a special top metal layer based on copper have been used in [84] to improve the quality factor of the inductor. Moreover, a CMOS compatible micro-electromechanical (MEM) technique to built air-core plastic deformation magnetic assembly (PDMA) inductors is utilized in [89]. Inductors in [90] use magnetic materials to improve the quality factor. A commercial product in [91] uses on-package inductors, but the capacitor is external. Package bondwires have a very good quality factor and have been employed to improve the efficiency of a buck converter in [92]. Nevertheless, this implementation may be unreliable due to the inductance variation of a bondwire. All these previous works utilize expensive post-fabrication techniques or high-cost special fabrication processes to produce a good quality inductor, while the proposed implementation utilizes a low-cost fabrication process.

6.2.4 Simulation Results

Figure 6.5 shows the layout of the buck converter. The size of the proposed converter is 2.5 mm x 4 mm. The output capacitor and the output inductor occupy more than 90% of the total area. The efficiency of the buck converter, including schematic and postlayout simulations, is presented in Figure 6.6. Process corner simulations performed on the voltage regulator yielded a variation in efficiency of

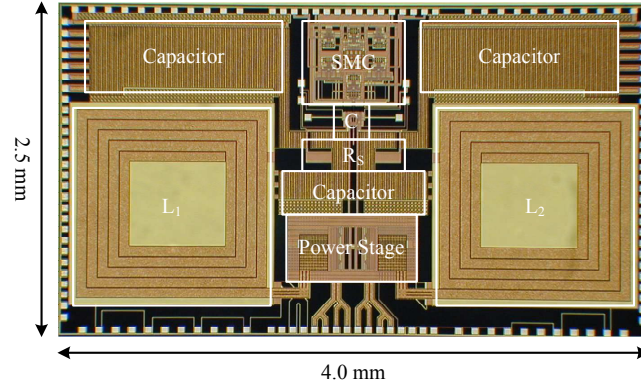


Figure 6.5: Layout of the proposed fully-integrated buck converter.

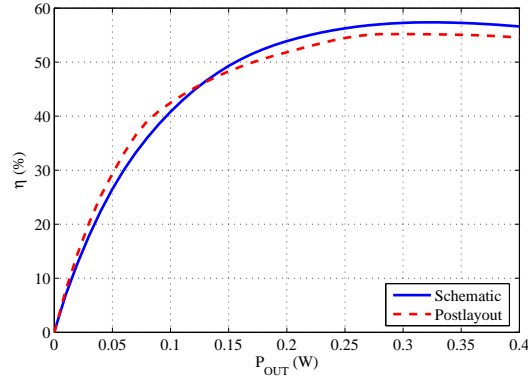


Figure 6.6: Efficiency versus P_{OUT} of the proposed buck converter.

only $\pm 5\%$. The anticipated Q_L of the designed inductor is approximately 3. The converter was also simulated for the hypothetical case of having a thicker top metal layer (higher Q_L). As Q_L increases, the equivalent series resistance drops, and the efficiency of the buck converter increments by more 10% from its original value as shown in Figure 6.7. The load transient response of the buck converter for a 100 mA step is shown in Figure 6.8.

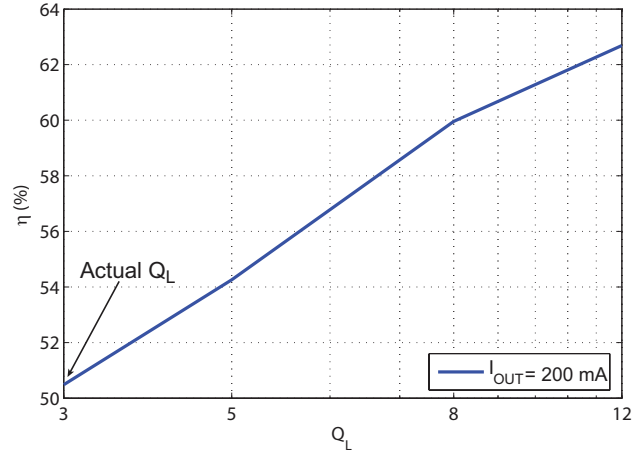


Figure 6.7: Efficiency versus Q_L .

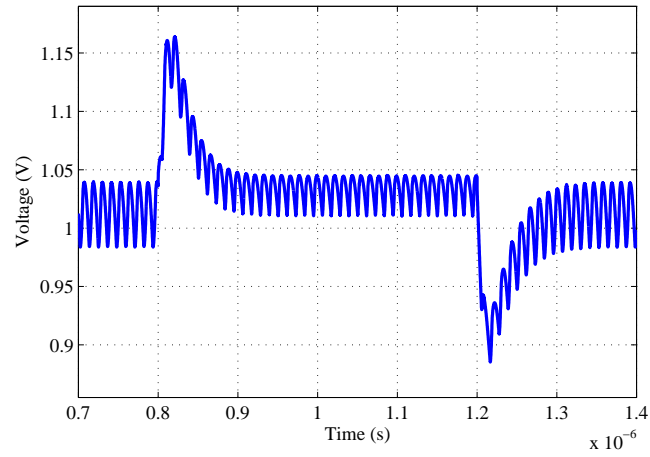


Figure 6.8: Output voltage variation for a current step from 100 mA to 200 mA and vice versa.

6.3 Buck Converter Power Stage Area Reduction

The implementation of multiple supply voltages in a given electronic product has become mandatory. A typical system as shown in Figure 6.9 requires the interaction of different subsystems, each one of them fabricated in a different technology process and with particular voltage specifications [2], [93]-[94], thus requiring multiple supply-voltage levels. There are circuits using newer technologies and lower voltage

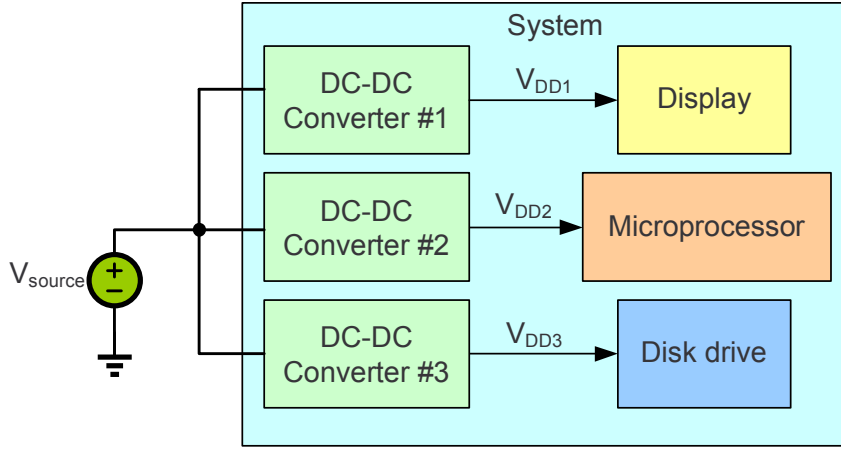


Figure 6.9: Multiple supplies on a typical system.

levels along with circuits using legacy power supplies and higher voltage levels [95]. Furthermore, using multiple supply voltages in digital circuits has significantly reduced dynamic power dissipation [96]. A dual power supply can reduce the dynamic power dissipation by employing a lower voltage in non-critical blocks and higher levels in critical paths, without compromising the overall circuit performance [2], [97]-[98].

Delivering multiple voltage levels requires the same number of switching converters, thus increasing component count and power stage area [99]. Previous solutions to this problem proposed sharing the output inductor in the low-pass filter to gener-

ate multiple output voltages [95], [100]. However, this method may present problems because one single inductor must store and deliver different levels of energy to each output. In this work, we propose a proof-of-concept dual-output buck converter with reduced number of switching elements in the power stage [93], [94] to demonstrate that the proposed solution can be feasible, reliable, cheap, and versatile.

6.3.1 Multiple-Output Buck Converter

A conventional synchronous buck converter architecture requires a pair of switches [3], thus generating n output voltages requires $2n$ switches. On the other hand, the proposed buck converter [93]-[94] implements only $n + 1$ switches for n outputs. The reduction in the number of switches reduces the amount of area and the number of external components, thus reducing the total cost of the system [93]-[94].

6.3.2 Dual-Output Operation

Figure 6.10 shows the basic schematic diagram of the dual-output buck converter and its modes of operation. The steady-state operation of the regulator has $n + 1$ subintervals for n outputs. For this specific case, a complete cycle of operation consists of three different subintervals.

During subinterval I, shown in Figure 6.10 (a), the switches T_1 and T_2 are closed, and switch T_3 is open. The current flows from the power supply through the inductors toward the output nodes. Since the converter requires $V_{OUT1} \geq V_{OUT2}$ for proper operation, the length of the first subinterval sets the duty cycle of V_{OUT2} . In subinterval II, illustrated in Figure 6.10(b), switch T_1 remains closed, switch T_2 opens, and switch T_3 closes. The duration of subinterval I plus that of subinterval II determines the duty cycle for V_{OUT1} ($D_1 \geq D_2$). Lastly, during subinterval III, depicted in Figure 6.10(c), switch T_1 opens, switch T_2 closes again, and switch T_3 remains closed. Figure 6.11 sketches the necessary non-overlapping signals to operate

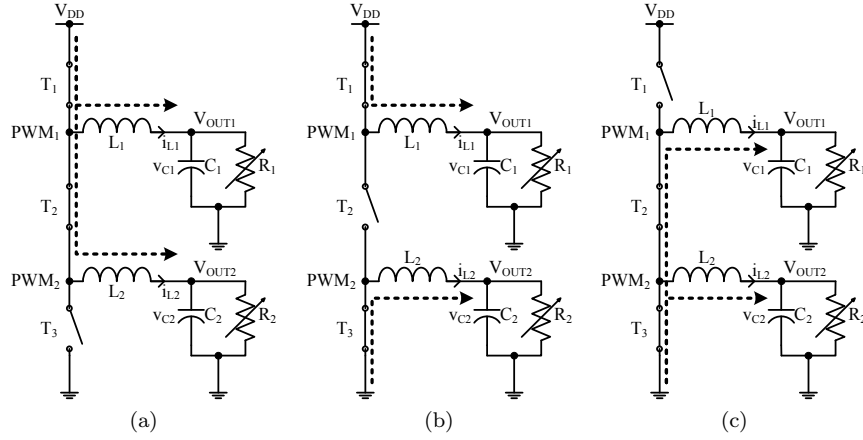


Figure 6.10: Schematic diagram of the dual-output buck voltage regulator and its operating modes (a) subinterval I (b) subinterval II and (c) subinterval III.

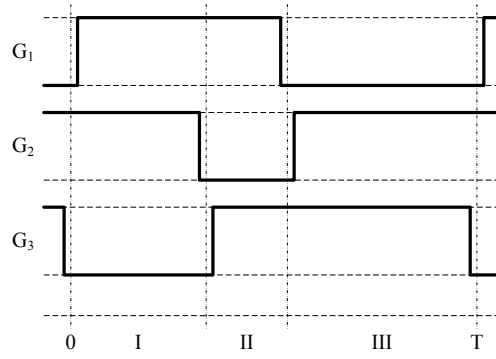


Figure 6.11: Sequence of non-overlapping operating signals applied to T_1 , T_2 , and T_3 , in the dual-output buck voltage converter.

the dual-output buck converter. Signals G_1 , G_2 , and G_3 , are applied to switches T_1 , T_2 , and T_3 , respectively.

The proposed converter was fabricated using $0.5 \mu\text{m}$ standard CMOS technology, operates with a voltage supply of 1.8 V, generates 1.2 V and 0.9 V, and supplies a maximum current of 200 mA (100 mA provided by each output). The switching frequency is 500 kHz. The current ripple Δi , and the voltage ripple Δv are 5% of the maximum current and 1% of the higher output voltage, respectively. The inductors

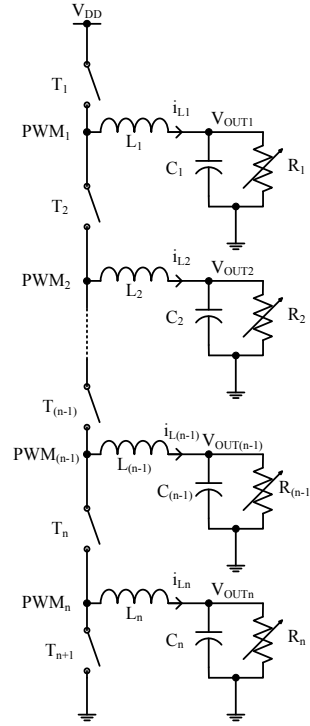


Figure 6.12: Single-input multiple-output converter.

and capacitors are the only off-chip components, and their values were calculated assuming continuous-conduction mode (CCM) steady-state operation [3].

6.3.3 Multiple-Output Operation

The proposed single-input dual-output converter can be extended into a single-input multiple-output converter if we keep stacking converters as shown in Figure 6.12. As in the case of the dual-output converter, $V_{OUT1} \geq V_{OUT2} \geq \dots \geq V_{OUT(n-1)} \geq V_{OUTn}$ for proper operation. The main advantage of multiple outputs would be the reduction of switches from $2n$ down to $n + 1$ for n outputs. On the other hand, the main disadvantage would be that V_{OUTn} would see substantial efficiency reduction due to all the switches connected in series. A trade-off between number of switches (losses) and efficiency should be considered when implementing

multiple outputs using this architecture.

6.3.4 Proposed Dual-Output Buck Converter Architecture

Figure 6.13 shows the proposed integrated dual-output converter architecture. The converter is a tracking system that minimizes the voltage errors (e_1 and e_2) between the reference signals (V_{REF1} and V_{REF2}) and the output signals (V_{OUT1} and V_{OUT2}) with the sliding mode controllers (SMC_1 and SMC_2). Then, two binary control signals (S_A and S_B) are combined using digital logic to generate the signals G_1 , G_2 , and G_3 , which control the output switches. Also, a sensing circuit at node PWM_2 generates a bootstrapped (BS) voltage signal to operate the middle switch. An output buffer (OB) drives the power switches and bootstrapped blocks. More details about the controller can be found in [21], [101]-[102].

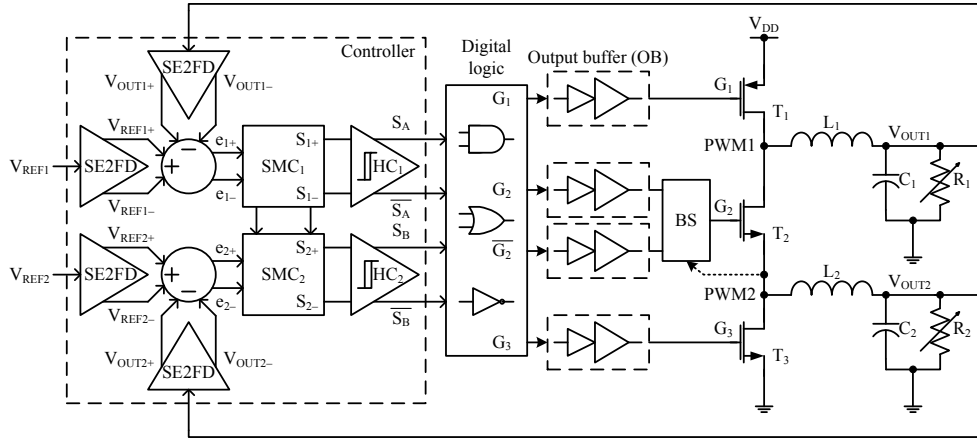


Figure 6.13: Block diagram of the proposed dual-output buck voltage converter.

6.3.5 Digital Logic Circuit

The digital logic synchronizes the binary signals (from comparators HC_1 and HC_2) and combines the two digital signals (S_A and S_B) to generate the three switch-

ing signals in Figure 6.11. Figure 6.14(a) shows a simplified representation of the digital-logic circuitry. The actual implementation of the logic circuitry includes delays elements and non-overlapping circuits for synchronization. The proposed synchronization method is compact and small. Moreover, it occupies only 4% of the overall silicon area.

The binary signals S_A and S_B determine the duty cycle of V_{OUT1} and V_{OUT2} , respectively. Assuming that $V_{OUT1} \geq V_{OUT2}$, PWM_1 and PWM_2 signals must follow the pattern shown in Figure 6.14(b), the duration of control signal G_1 corresponds to the duty cycle of V_{OUT1} , e.g., $G_1 = S_A$.

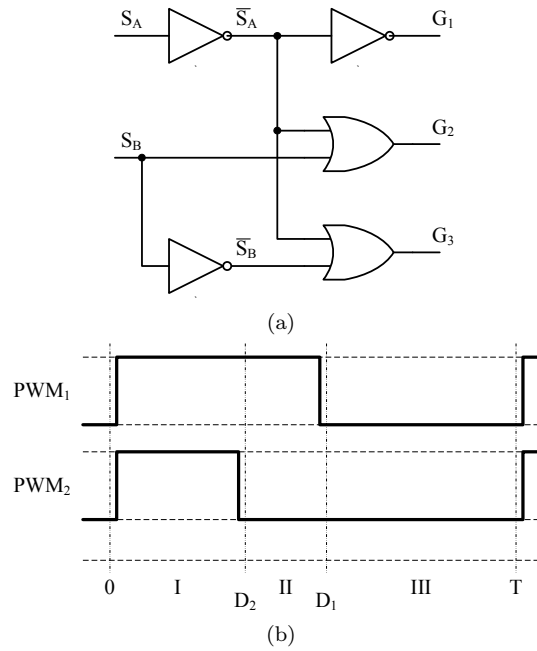


Figure 6.14: (a) Simplified digital logic to generate G_1 , G_2 , and G_3 and (b) Buck converter switching signals PWM_1 and PWM_2 .

The middle switch T_2 is controlled by G_2 with a logical OR operation between signals $\overline{S_A}$ and S_B ($G_2 = \overline{S_A} + S_B$) because it must be closed whenever V_{OUT1} is

connected to ground or V_{OUT2} is connected to the power supply, as shown previously in Figure 6.11.

The last switch T_3 is triggered by G_3 with a logical OR operation between the signals $\overline{S_A}$ and $\overline{S_B}$ ($G_3 = \overline{S_A} + \overline{S_B}$) because it must be closed only when either output is connected to ground, as illustrated previously in Figure 6.11.

6.3.6 Output Power Stage

The output power stage must provide enough drive capability for the digital-gate control signals G_1 , G_2 , and G_3 to trigger the power switches.

6.3.6.1 Output Buffer Stage and Output Switches

The output buffer must minimize the dynamic power dissipation without jeopardizing the propagation delay, must reduce the short-circuit current during transitions, and must minimize the CMOS on-resistance R_{on} [64]-[66]. The output buffer is designed assuming that the voltage regulator will work at medium load most of the time. The calculations yield a tapering factor $T = 24$, number of inverters $N = 4$, and $R_{on} = 307 \text{ m}\Omega$. The size of the PMOS output switch is $W_{T1} = 55.08 \text{ mm}$ with $L_{T1} = 0.6 \text{ }\mu\text{m}$. The size of NMOS transistors W_{T2} and W_{T3} is one third of PMOS transistors [64]-[66] to achieve the same R_{on} as the PMOS. If the conventional solution with four power transistors is designed to have the same R_{on} , the dimensions of the PMOS transistors would be $W_{Tp} = 55.08 \text{ mm}$ with $L_{Tp} = 0.6 \text{ }\mu\text{m}$ and the dimensions of the NMOS transistors would be $W_{Tn} = 18.33 \text{ mm}$ with $L_{Tn} = 0.6 \text{ }\mu\text{m}$. Hence, an estimated area reduction of 37.5% on the power transistors could be achieved with the proposed solution when compared with the conventional one.

6.3.6.2 Bootstrapping Circuit

Power switch T_2 in Figure 6.13 requires a bootstrapping circuit to turn it on and off completely. Figure 6.15 shows the transistor level implementation of the bootstrapping circuit. A clock multiplier that consists of transistors M_1 and M_2

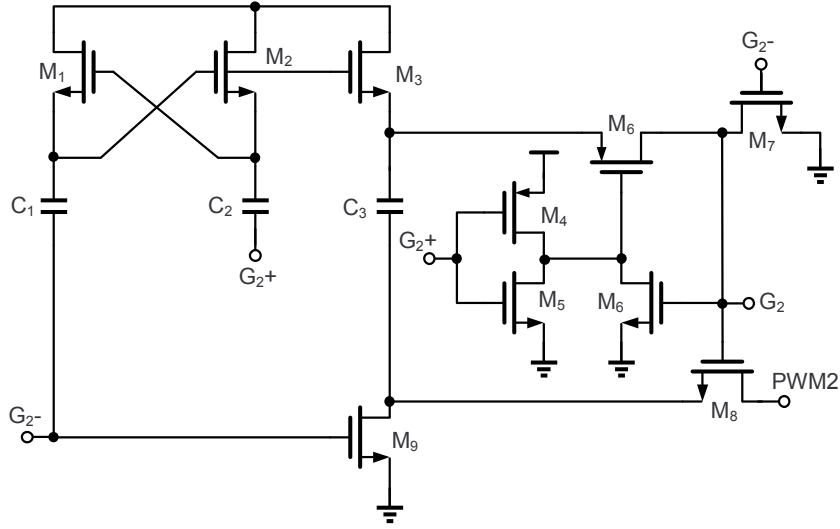


Figure 6.15: Transistor level implementation of the bootstrapping circuit.

and capacitors C_1 and C_2 charges capacitor C_3 by enabling transistor M_3 [103]. Capacitors C_1 and C_2 are implemented on-chip, and each one has a value of 8 pF. Capacitor C_3 is implemented with an off-chip component of 1 nF since it needs to be large enough to charge power transistor T_2 . The digital signals $G_{2\pm}$ are generated by the digital logic and they act as the clocking signals of the circuit. Signals G_2 and $PWM2$ are connected to the gate and source of power transistor T_2 , correspondingly. In our design, the maximum gate-source gate-drain of the bootstrapping transistor(s) is 3.6 V, which is less than the nominal supply of 5 V for this process.

6.3.7 Simulation and Experimental Results

The proposed dual-output buck converter was fabricated in 0.5 μm standard CMOS technology. Figure 6.16 shows the IC micrograph with all main blocks highlighted: the analog controller (SE2FD converters, SMC_1 and SMC_2 , and decision circuits HC_1 and HC_2); the digital logic; and the output stage (output buffers (OB), the bootstrapping (BS) circuit, and output switches (T_1 , T_2 , and T_3).

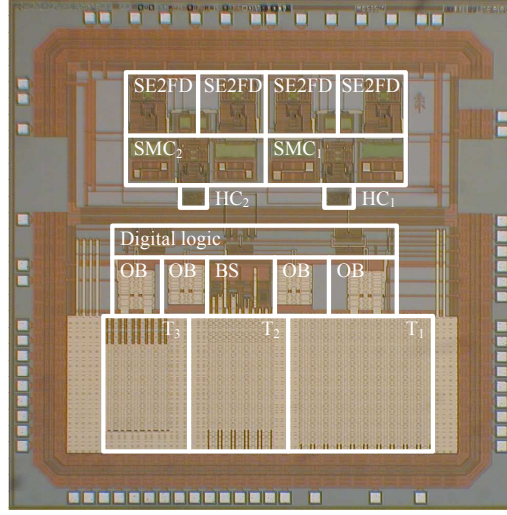
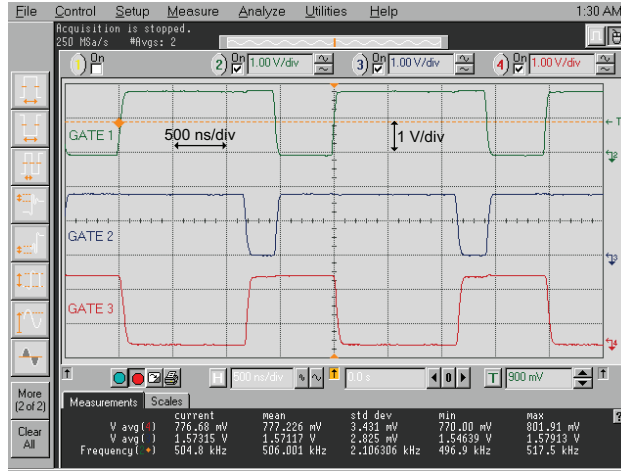


Figure 6.16: Dual-output buck voltage regulator IC micrograph.

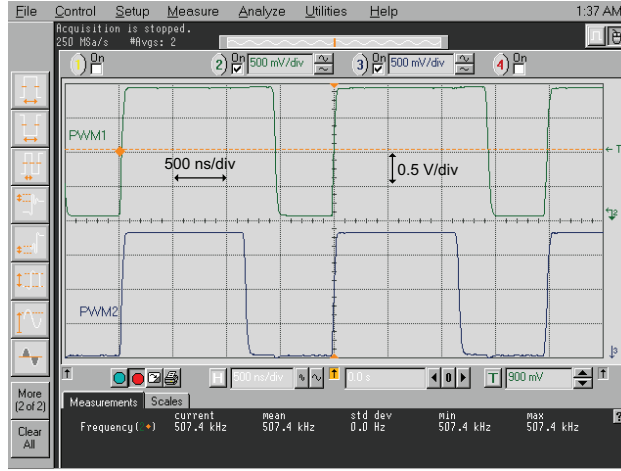
6.3.8 Steady-State Operation of the System

6.3.8.1 Control Signals

Figure 6.17(a) shows the measured control signals G_1 , G_2 , and G_3 that operate the output switches T_1 , T_2 , and T_3 . Note that they follow the same pattern as the operational signals sketched previously in 6.11. The switching frequency is approximately 500 kHz. Figure 6.17(b) displays the modulated signals $PWM1$ and $PWM2$.



(a)



(b)

Figure 6.17: Measured (a) control signals G_1 , G_2 , and G_3 and (b) pulse-width modulated signals.

The measured duty cycles for V_{OUT1} and V_{OUT2} are 71% and 55%, respectively.

6.3.8.2 Power Efficiency

Figure 6.18 plots the efficiency measurements. The maximum efficiency of the dual-output buck converter is 88%. The efficiency is maximum when the output voltage V_{OUT1} is set to medium load condition and the output voltage V_{OUT2} is draining low current. The efficiency of the dual-output buck voltage converter is

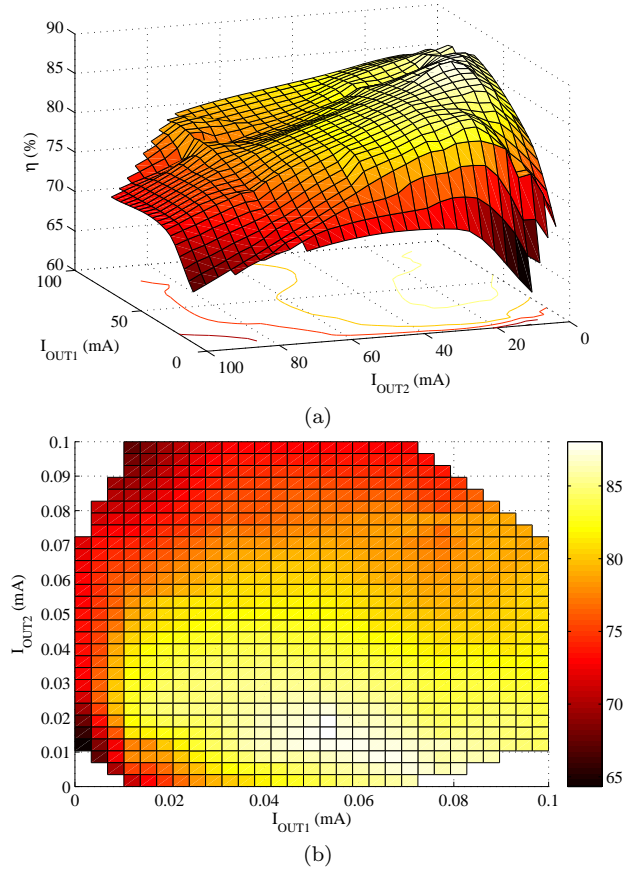
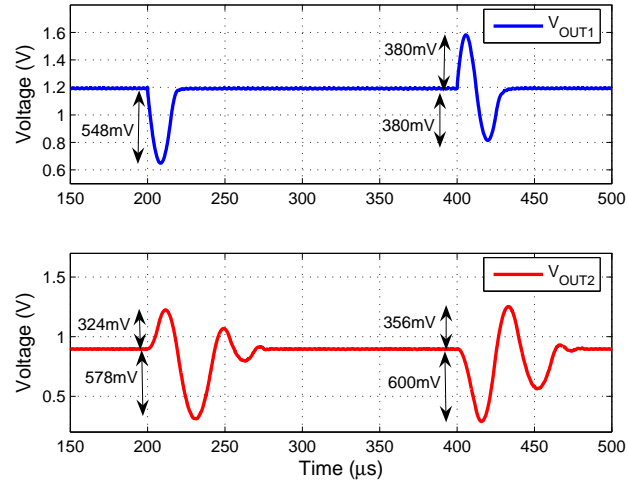


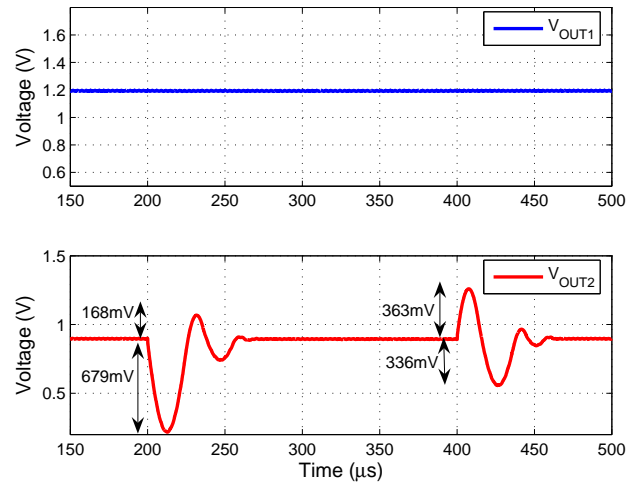
Figure 6.18: (a) Power efficiency measurements of the dual-output buck voltage versus both output currents and (b) top view of (a).

always higher when the output V_{OUT1} drains more current than output V_{OUT2} . Figure 6.18(a) shows the power efficiency versus both output currents and Figure 6.18(b) shows a top view of the same plot.

The proposed converter provides better efficiency when I_{OUT2} is low because the current has to travel across two switches instead of one as in a typical architecture. This increases the ON-resistance losses, and therefore, the efficiency drops when I_{OUT2} increases; hence, the dual-output converter provides its maximum efficiency when I_{OUT1} is at medium loads and I_{OUT2} is at light loads.



(a)



(b)

Figure 6.19: Load regulation when (a) 100 mA step is applied to I_{OUT1} while I_{OUT2} is fixed at 0 mA and (b) I_{OUT1} is fixed at 0 mA while 100 mA step is applied I_{OUT2} .

6.3.9 Transient Operation of the System

Figure 6.19 shows the post-layout load regulation response of the system. Figure 6.19(a) shows the load regulation effect when a 100 mA current step is applied to V_{OUT1} . Here, the cross-regulation effect on V_{OUT2} is noticeable because switch T_1 is only controlled by the top converter, hence affecting the second converter. On the other hand, Figure 6.19(b) shows the load regulation effect when a 100 mA current step is applied to V_{OUT2} . Here, there is no cross-regulation effect on V_{OUT1} because the top switch doesn't see any load effect since I_{OUT1} doesn't change. However, V_{OUT2} takes longer recovery time because switch T_1 is independent of I_{OUT2} .

The load regulation can be improved significantly if the size of the output filter is optimized for a given load step. The output inductor can be reduced (while the output capacitor is increased) to improve the transient response of the dual-output converter, as long as the same cut-off frequency is maintained. The proposed design was optimized not for a transient response but for a minimum output ripple.

Figure 6.20 shows the line regulation response of the system. As can be seen, V_{OUT1} only deviates around 10 mV when V_{IN} changes from 1.8 V to 2.5 V. In all cases of load and line regulation, the proposed converter is stable when a full-range step (either current or voltage) is applied. Figure 6.21 presents two cases of the measured results. Figure 6.21(a) shows the case when V_{OUT1} presents a step of 25 mA, while V_{OUT2} is at high load configuration, i.e., 60 mA, and Figure 6.21(b) illustrates the case when V_{OUT1} is kept at high load (60 mA), while a 25 mA current step is applied to V_{OUT2} . A current step in V_{OUT2} affects the controller's transient response more than a current step in V_{OUT1} . This phenomenon was expected because the path of the output current is shared by both outputs, but controlled only by the gate signal G_1 .

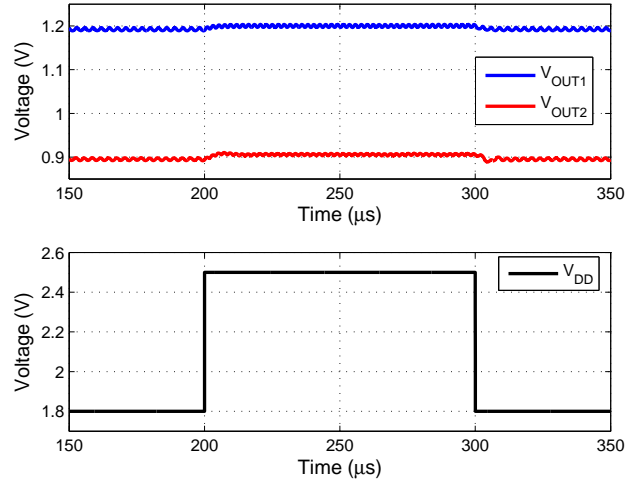


Figure 6.20: Line regulation with V_{IN} (V_{DD}) step from 1.8 V to 2.5 V (refer to Figure 6.13).



Figure 6.21: (a) 25 mA step is applied to I_{OUT1} while I_{OUT2} is fixed at 60 mA and (b) I_{OUT1} is fixed at 60 mA while 25 mA step is applied I_{OUT2} .

Table 6.2: Comparison of dual-output buck voltage regulators

Design	[99]	[100]	This work
V_{DD} (V)	3.0	3.6	1.8
V_{OUT1} (V)	2.0	3.3	1.2
V_{OUT2} (V)	1.0	1.8	0.9
I_{MAX} (mA)	55	200	200
η (%)	89	85	88
L (μ H)	440, 440	22	82,90
C (μ F)	0.22, 0.22	35, 35	0.83, 1.11
Switches	4	4	3
Δv (mV)	40, 40	31, 24	12, 9
f_s (kHz)	500	1000	500
P_Q (μ W)	411.6	-	188.6
Area (mm^2)	4.57	2.43	2.19
CMOS process (μm)	-	0.35	0.5

The system is stable and quickly converges to the reference voltages, as expected. The dual-output buck voltage converter performs better when $I_{OUT1} \geq I_{OUT2}$, because the branch connected to the power supply is shared by the two output nodes. Therefore, when V_{OUT2} needs to supply a large amount of current quickly, the current path may be disconnected because it is controlled by the duty cycle of V_{OUT1} .

The switches in the proposed topology have higher RMS current than the conventional converter because each switch carries current corresponding to both outputs [93]-[94]. This means that the switches must be optimized if both outputs must be supplied with full load. However, both outputs are seldom at full load simultaneously, and even then, the duration of such a condition is short. Thus, the switches in the proposed converter need not be sized for the maximum load capabilities of both outputs. Table 6.2 summarizes the overall characteristics of the proposed converter, and compares them to previously reported dual-output regulators. Even though the voltage ratings are different, the proposed converter can deliver the same output

current as previous works but consumes less static power P_Q . Moreover, the value of the inductors in the proposed architecture can be further reduced if a larger current ripple can be tolerated, thereby reducing cost and space.

Additionally, the reduction of one switch with respect to conventional architectures, saves silicon area if the output stage is optimized for medium load applications. The proposed dual architecture could also reduce printed circuit board area because it requires only one input filter, whereas the conventional solution requires two, one for each individual buck converter.

6.4 Buck Converter Compensator Area Reduction

As already mentioned in Section 5, buck converters operate in a closed loop fashion to minimize the effect of load perturbations and/or input voltage variations, which could affect the output voltage [3]. However, this closed loop operation makes the buck converter stability a concern. Figure 6.22 shows the closed loop block diagram of a voltage mode buck converter which includes a compensator, a carrier signal generator, a comparator, a power stage, and an output filter. When analyzing

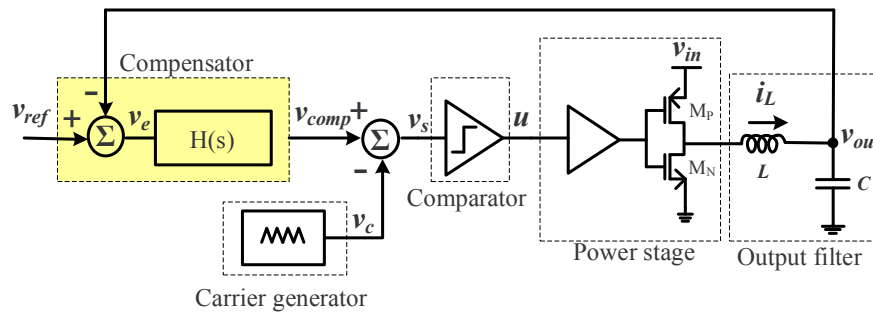


Figure 6.22: Block diagram of a voltage mode PWM buck converter.

the stability of the loop, the combination of the carrier signal generator, comparator,

and power stage is typically referred as the modulator and its gain is often assumed to be constant [52]-[53]. A compensator is necessary to boost the loop phase margin to counteract the effect of the output filter's complex poles located at $f_{LC} = 1/(2\pi\sqrt{LC})$.

A Type-III voltage mode compensator is typically employed to achieve high crossover frequency and good phase margin in applications where fast transient response and output filter capacitors with small R_{ESR} are required [54]. The conventional Type-III compensation requires large capacitor and resistor values to generate large time constants; which make their on-chip integration difficult. Due to area constraints in many cases the Type-III compensation is completely [104] or partially [105] implemented with external passive components. This may provide some flexibility to costumers at the expense of increasing the PCB area and system cost [106]. In [107], a buck voltage regulator with an interesting on-chip pseudo-Type-III compensation was proposed. This compensator was synthesized by adding a high-gain path and a secondary moderate-gain path at the inputs of the PWM comparator. Even though, this topology significantly reduces the area and power consumption of the compensator when compared with the conventional approach; the compensator's quiescent current is still $30\ \mu\text{A}$, and the total compensation capacitance is $110\ \text{pF}$. The compensator's area becomes more critical in buck converters implemented in sub-250nm technologies, where the maximum current is in the order of hundreds of mA, because it is comparable to the power stage's area.

In this section, we propose a compensation scheme that employs a cascade combination of Gm-RC and Active-RC blocks to reduce the compensator's area while consuming low quiescent power and still achieving high performance. As a result, the total active area is significantly reduced.

6.4.1 Proposed Compact Compensation

The block and circuit diagrams of the proposed compensator are shown in Figure 6.23. The proposed topology can be divided in two sections: Gm-RC and Active-

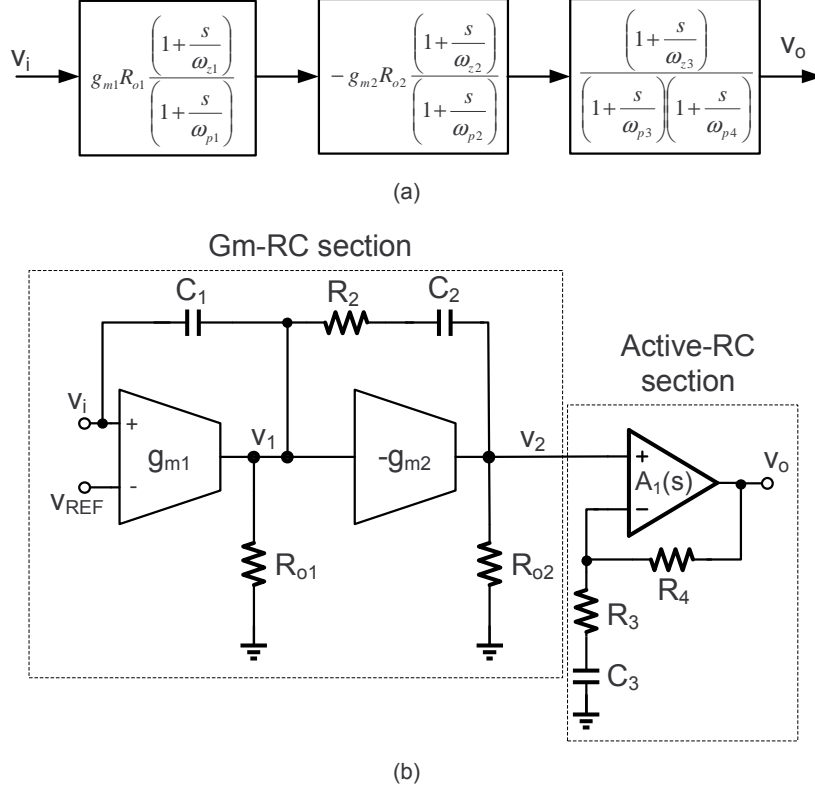


Figure 6.23: (a) Block and (b) circuit diagrams of the proposed compensator.

RC. The Gm-RC section is implemented with a two-stage operational transconductance amplifier, where g_{mi} and R_{oi} (for $i = 1, 2$) represent the transconductances and output resistances of each stage, respectively. C_1 and C_2 are compensation capacitors and R_2 is a compensation resistor. The transfer function of the Gm-RC section

can be expressed as:

$$\frac{V_2(s)}{V_i(s)} \cong -A_{DC} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p2}} + 1\right)}. \quad (6.7)$$

where

$$A_{DC} = g_{m1}R_{o1}g_{m2}R_{o2}, \quad \omega_{z1} = \frac{g_{m1}}{C_1}, \quad \omega_{z2} = \frac{1}{R_2C_2},$$

$$\omega_{p1} = \frac{1}{R_{o1}g_{m2}R_{o2}C_2}, \quad \omega_{p2} = \frac{g_{m2}}{C_1}.$$

The zero (ω_{z2}), given by R_2C_2 , is used to cancel the effect of the high frequency pole (ω_{p2}) given by g_{m2}/C_1 . Hence, (6.7) can be simplified to:

$$\frac{V_2(s)}{V_i(s)} \cong -A_{DC} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right)}. \quad (6.8)$$

The Active-RC section is implemented with a resonator circuit that consists of two resistors R_3 and R_4 , a capacitor C_3 , and an amplifier $A_1(s)$. Assuming $A_1(s) \cong \text{GBW}/s$, the transfer function of the Active-RC section can be expressed as,

$$\frac{V_o(s)}{V_2(s)} \cong \frac{\left(\frac{s}{\omega_{z3}} + 1\right)}{\left(\frac{s}{\omega_{p3}} + 1\right) \cdot \left(\frac{s}{\omega_{p4}} + 1\right)} \quad (6.9)$$

where

$$\omega_{z3} = \frac{1}{(R_3 + R_4)C_3},$$

$$\omega_{p3} = \frac{1}{R_3C_3}, \quad \omega_{p4} \cong \text{GBW} \frac{R_3}{R_3 + R_4}.$$

where GBW is the gain bandwidth product of $A_1(s)$.

The transfer function of the proposed compensator is given by the multiplication

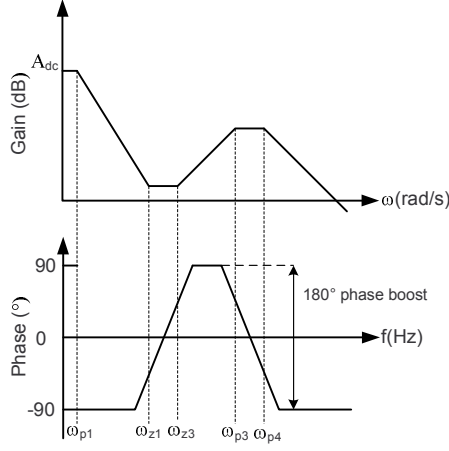


Figure 6.24: Proposed compensator Bode plot.

of the transfer function of the Gm-RC and Active-RC sections:

$$H(s)_{Prop} = \frac{V_o(s)}{V_i(s)} = -A_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \cdot \left(\frac{s}{\omega_{z3}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p3}} + 1\right) \cdot \left(\frac{s}{\omega_{p4}} + 1\right)}. \quad (6.10)$$

In this design, the poles and zeros are placed as suggested in [52]:

- The first zero, $\omega_{z1} = g_{m1}/C_1$, is placed at $\frac{\omega_{LC}}{2} = \pi f_{LC} = \frac{1}{2\sqrt{LC}}$.
- The second zero, $\omega_{z2} = 1/((R_3+R_4)C_3)$, is placed at $\omega_{LC} = 2\pi f_{LC} = \frac{1}{\sqrt{LC}}$.
- The first pole, $\omega_{p1} = \frac{1}{R_{o1}g_{m2}R_{o2}C_2}$, is placed at the location of the low-frequency pole in the conventional Type-III implementation.
- The second pole, $\omega_{p3} = \frac{1}{R_3C_3}$, is placed at $\frac{\omega_s}{2} = \pi f_s$.
- The third pole, $\omega_{p4} = 2\pi GBW \cdot \left(\frac{R_3}{R_3+R_4}\right)$, is placed at $\omega_{ESR} = 2\pi f_{ESR} = \frac{1}{R_{ESR}C_L}$, where C_L is the output filter's capacitor.

The Bode plot of the proposed compensation scheme is shown in Figure 6.24. The poles and zeros of the proposed compensation scheme are placed at similar

frequencies as the poles and zeros of the conventional Type-III compensation. Figure 6.25 depicts the analytical expression given by (6.10) and the simulated open loop frequency response of the buck converter with the proposed compensator. The

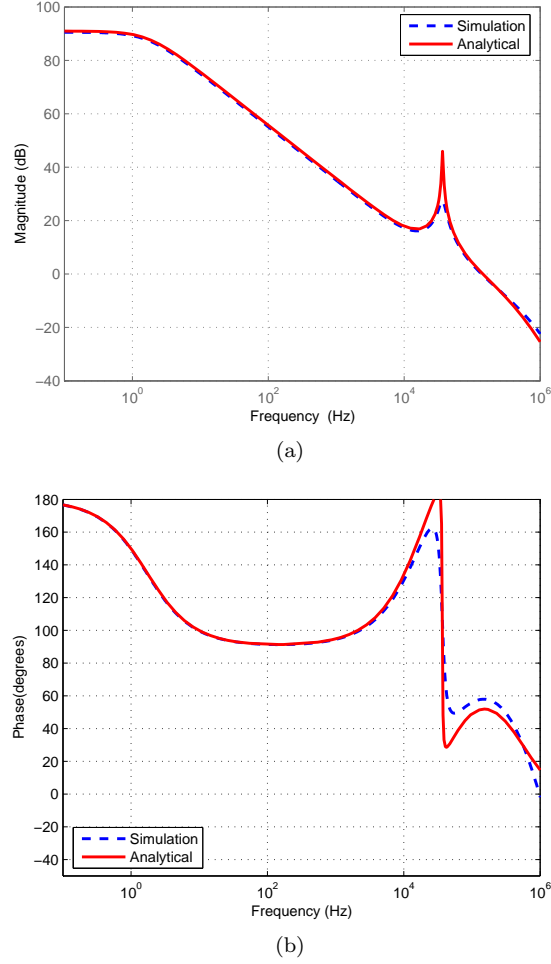


Figure 6.25: Buck converter open loop frequency response with the proposed compensator (a) gain (b) phase.

phase margin (ϕ_m) of the loop versus process corners for different temperatures is shown in Figure 6.26. As can be observed, the worst variation of ϕ_m is only 2.3° ,

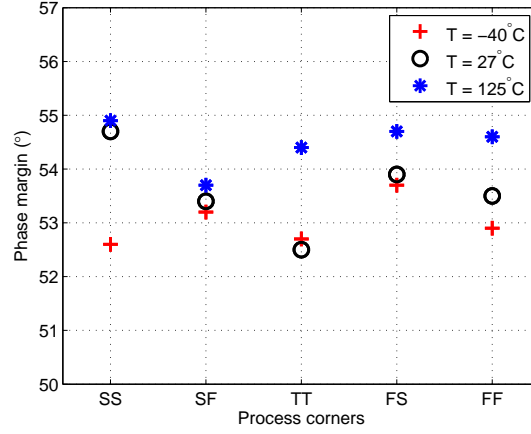


Figure 6.26: Loop phase margin with proposed compensator versus process corners.

as the minimum and maximum phase margin is 52.6° and 54.9° , respectively. Table 6.3 shows the component's values for the conventional Type-III and the proposed compensation topologies for an identical technology and a similar loop transfer function. As can be seen from Table 6.3, the total compensation capacitance of the

Table 6.3: Component's value of compensation implementations

Parameters	Conventional	Proposed
R_1	400 k Ω	N/A
R_2	236 k Ω	40 k Ω
R_3	29 k Ω	33 k Ω
R_4	N/A	440 k Ω
C_1	0.4 pF	1.2 pF
C_2	40 pF	1.7 pF
C_3	11 pF	10.0 pF
Total Resistance	665 k Ω	513 k Ω
Total Capacitance	51.4 pF	12.9 pF
Compensator's Area	0.0502 mm ²	0.0267 mm ²
Total Active Chip Area	0.1560 mm ²	0.1325 mm ²

proposed compensator is approximately 4 times smaller than the conventional compensator. While the total compensation resistance of the proposed topology is 1.3 times smaller than the conventional one. Figure 6.27 shows the area distribution of a buck converter implemented with: (a) the conventional Type-III compensation and (b) the proposed compensation scheme in $0.18\ \mu\text{m}$ CMOS standard technology. Both buck converters are implemented with the same power stage, comparator, and

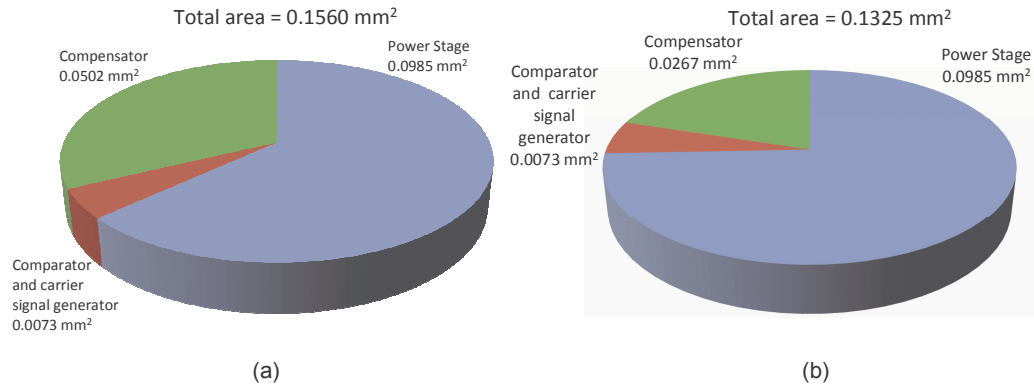


Figure 6.27: Area distribution of a buck converter implemented with: (a) conventional Type-III compensator and (b) proposed compensator.

carrier signal generator. The total area occupied by the conventional Type-III compensator and proposed compensator are $0.1560\ \text{mm}^2$ and $0.1325\ \text{mm}^2$, respectively. The proposed compensator occupies approximately 53% of the conventional Type-III compensator area. The buck converter implemented with the proposed compensator occupies approximately 85% of the area occupied by the buck converter implemented with the conventional Type-III compensation. Additional area can be saved if capacitor C_3 is implemented with a MOS capacitor instead of a MIM capacitor; and/or the resistor R_2 is implemented with a transistor operating in the triode region. Both

where $g_{m_{M_C}}$ is the transconductance (operating in saturation) of the composite transistor. Thus, the effective transconductance is reduced by $M + 1$ when compared with the one before current splitting [109]. Parameter g_{m2} is implemented as a common source stage, and it is the transconductance of transistor M_3 :

$$g_{m2} = g_{m,M3} = \sqrt{2I_{D,M3}\mu_n C_{ox} \left(\frac{W_{M3}}{L_{M3}} \right)} \quad (6.12)$$

where $I_{D,M3}$, μ_n , C_{ox} are the drain current, mobility, and oxide capacitance of transistor M_3 , respectively. W_{M3} and L_{M3} are the dimensions of transistor M_3 . The total current consumption of the Gm-RC section is approximately $1.8 \mu\text{A}$. This section of the compensator can be designed using the following procedure:

1. Select a value for g_{m1} and then calculate C_1 by placing f_{z1} at $f_{LC}/2$:

$$C_1 = 2g_{m1} \cdot \sqrt{LC} \quad (6.13)$$

2. Set $g_{m1}R_{o1}g_{m2}R_{o2}$ equal to the DC gain of the error amplifier in the conventional Type-III error amplifier.
3. Calculate C_2 by placing f_{p1} at the low-frequency pole ($f_{p,dom}$) of the conventional Type-III implementation:

$$C_2 = \frac{1}{2\pi R_{o1}g_{m2}R_{o2}f_{p,dom}} \quad (6.14)$$

6.4.2.2 Active-RC Section

Amplifier A_1 is implemented using the two-stage amplifier with Miller compensation. The amplifier's GBW is used as a design parameter. This section of the

compensator can be designed using the following procedure:

1. Select a value for R_3 and then calculate C_3 by placing f_{p3} at $f_s/2$:

$$C_3 = \frac{1}{\pi f_s R_3} \quad (6.15)$$

2. Calculate R_4 by placing zero f_{z3} at f_{LC} :

$$R_4 = R_3 \cdot \left(\frac{f_s}{2f_{LC}} - 1 \right) \quad (6.16)$$

3. Calculate GBW by placing f_{p4} at f_{ESR} :

$$GBW = f_{ESR} \cdot \left(1 + \frac{R_4}{R_3} \right) \quad (6.17)$$

The amplifier has a DC gain of 72.9 dB, a GBW (g_{m1}/C_c) of 18.9 MHz, and consumes a quiescent current of 7 μ A. The Miller capacitor can be calculated using the following equation:

$$C_m = \frac{g_{m,A1}}{2\pi GBW} \quad (6.18)$$

where $g_{m,A1}$ is the transconductance of the amplifier's first stage. The value of the Miller capacitor is only 130 fF in this design.

6.4.2.3 Comparator

A hysteretic comparator [76] was utilized in the modulator to improve the noise immunity of the system. Figure 6.29 shows the transistor level implementation of the comparator which consists of two stages: the input stage with positive feedback and the output stage. The first stage consists of transistors M_1 - M_3 . The hysteresis

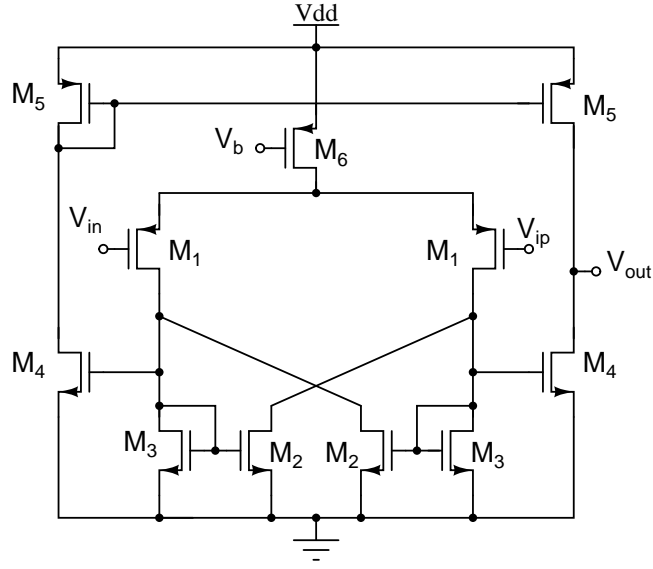


Figure 6.29: Comparator transistor level implementation.

window is given by [75]:

$$V_{hys} = 2\sqrt{\frac{I_{M6}}{K_p}} \left(\frac{1 - \sqrt{\alpha}}{\sqrt{1 + \alpha}} \right)$$

where

$$\alpha = \frac{W_2 L_3}{W_3 L_2} \quad (6.19)$$

The second-stage(M_4 - M_5) is required to achieve nearly rail-to-rail output voltage swing and provide a Class-AB type of driving capability. The current consumption is approximately $1.3 \mu\text{A}$.

6.4.2.4 Carrier Signal Generator

The carrier signal generator, shown in Figure 6.22, was implemented using the circuit shown in Figure 6.30. The frequency of this circuit is determined by the input square waveform which operates at 1 MHz with 50% duty cycle (D) and it is

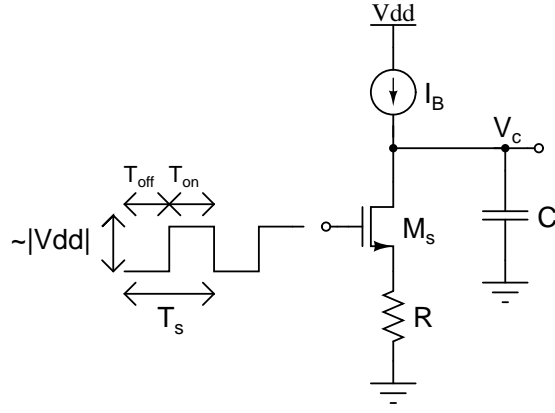


Figure 6.30: Carrier signal generator implementation.

generated externally in this prototype. During T_{off} , transistor M_s is off, and the current source I_B charges the output capacitor C linearly. During T_{on} , transistor M_s is on, and C is discharged exponentially through R . The peak-to-peak voltage amplitude of the carrier signal can be expressed as,

$$V_{c,pp} = \frac{T_{off} I_B}{C}, \quad (6.20)$$

where

$$T_{off} = (1 - D) T_s. \quad (6.21)$$

Applying capacitor charge balance [3], the average voltage of the carrier of the carrier signal can be found to be:

$$V_{c,avg} = \frac{R I_B}{D}, \quad (6.22)$$

where D is the duty cycle of the input square waveform. It is important to choose an appropriate average voltage since it sets the input common mode voltage of the comparator and the output common mode voltage of the compensator circuit.

If the value of the chosen R is large enough, a quasi-linear negative slope is

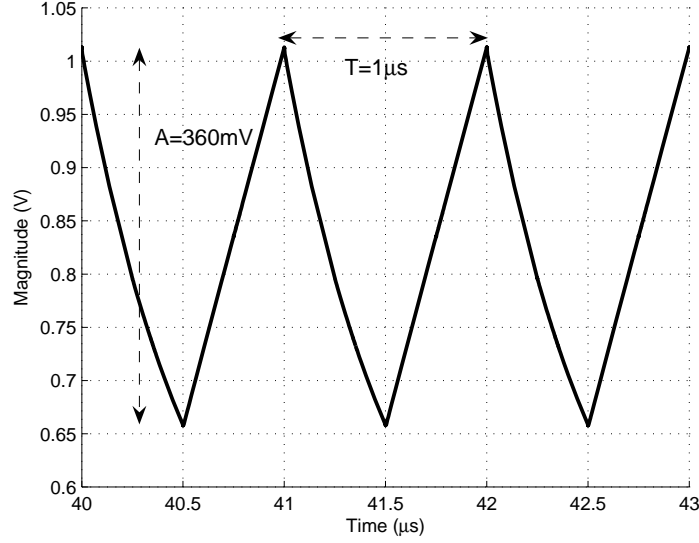


Figure 6.31: Carrier signal waveform.

achieved as shown in Figure 6.31. The THD of the waveform shown in Figure 6.31 is approximately 13.36 dB, while the THD of an ideal triangle wave is 12.22 dB. The values of I_B , R , and C were chosen to be $2 \mu\text{A}$, $213.5 \text{ k}\Omega$, and 2.8 pF , respectively. For the chosen values, $V_{c,pp}$ and $V_{c,avg}$ are approximately 357 mV and 854 mV, respectively. The modulator gain G_M can be approximated as [3], [52]-[53],

$$G_M = \frac{V_{in}}{V_{c,pp}}, \quad (6.23)$$

where V_{in} is the input voltage of the buck converter (see Figure 6.1). For an input voltage of 1.8 V, G_M is approximately 14 dB. The proposed carrier signal generator can be designed using the following procedure:

1. Select the peak-to-peak amplitude for the carrier signal generator ($V_{c,pp}$) to

achieve a desired modulator gain:

$$V_{c,pp} = \frac{V_{in}}{G_M} \quad (6.24)$$

2. Select a value for I_B and then calculate C using the following equation (this assumes that T_s and D were previously defined):

$$C = \frac{(1 - D) T_s I_B}{V_{c,pp}} \quad (6.25)$$

3. Select the desired common mode voltage $V_{c,avg}$ and calculate R :

$$R = \frac{DV_{c,avg}}{I_B} \quad (6.26)$$

6.4.2.5 Power Stage Implementation

Figure 6.32 shows the implemented power stage block diagram. The power FETs (M_P and M_N) were designed to minimize the conduction losses by reducing the CMOS on-resistance R_{on} . The dimensions of the PMOS power switch (M_P) are $W = 25000 \mu\text{m}$ and $L = 0.18 \mu\text{m}$, and the dimensions of the NMOS power switch (M_N) are $W = 12500 \mu\text{m}$ and $L = 0.18 \mu\text{m}$.

The driver stage was optimized to minimize the gate drive power losses without degrading the propagation delay, and the short circuit current was reduced with a non-overlapping configuration [111]. The functions of drive and non-overlapping time are implemented separately; the buffers are in the forward path, and the delay elements are in the feedback path as shown in Figure 6.32. By doing this, the buffers can be designed in a compact fashion with low power consumption and the delay elements can be designed independently without affecting the delay of the

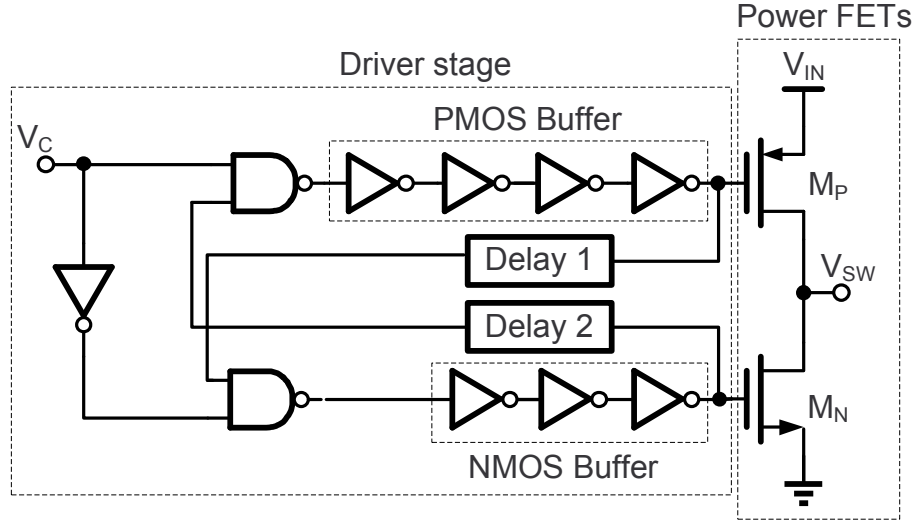


Figure 6.32: Power stage block diagram.

forward path. The non-overlapping time should be small enough that it does not degrade the overall efficiency but large enough to deal with process variation [112]. Based on simulation results and considering these design trade-offs, a non-overlapping time of 8 ns was chosen. Delay 1 element was implemented with 6 inverters and Delay 2 element with 7 inverters. Even with the delay block placed in the feedback path, the forward driving path should be designed taking into consideration the trade-off between the delay and power consumption. For the smallest propagation delay, the optimized scale factor between stages is mathematically equal to Euler's number [79]; however, it requires an impractical number of stages which increases area and switching power consumption. Therefore, for the PMOS driver, a scale factor of 20 was used for the last buffer stage, and 7, 6, and 5 for the previous stages, respectively. For the NMOS driver, the scale factors are: 15, 10, and 8 for the third, second, and first inverter, correspondingly. As a result, the gate driver power losses are reduced and the system achieves high efficiency over a large output power range.

6.4.2.6 Output Filter Implementation

The second-order low-pass filter consists of two capacitors in parallel of $4.7 \mu\text{F}$ with an R_{ESR} of $10 \text{ m}\Omega$ each, and an inductor of $2 \mu\text{H}$. The transfer function of the output filter is given by:

$$H(s)_{filter} = \frac{\frac{s}{\omega_z} + 1}{\frac{s^2}{\omega_o^2} + \frac{1}{\omega_o Q}s + 1} \quad (6.27)$$

where

$$\omega_o = \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_{ESR}C}, \quad Q = \frac{1}{R_{ESR} + 2R_{DCR}}\sqrt{\frac{L}{C}} \quad (6.28)$$

These components generate complex poles at a frequency similar to the ones generated by an output filter with a capacitor of $4.7 \mu\text{F}$ and an inductor of $4.7 \mu\text{H}$ [107]. However, the proposed component values reduce the output impedance of the buck converter [106], [113] and as result, for given current step during load transient, the amplitude of the voltage dips and surges are smaller with the proposed configuration.

6.4.3 Experimental Results

The proposed buck converter was fabricated in $0.18 \mu\text{m}$ CMOS standard technology. The chip prototype was encapsulated in a QFN 28 package. Figure 6.33 shows the die micrograph of the fabricated buck converter where blocks I, II, and III correspond to the compensator, comparator and carrier signal generator, and power stage, respectively. The total active area occupied by the buck converter is 0.1325 mm^2 . The prototype was tested for an input voltage of 1.8 V and an output voltage of 0.9 V . Table 6.4 summaries the performance of the prototype and compares it to that of the state-of-the-art voltage mode buck converters operating at 1 MHz switching frequency.

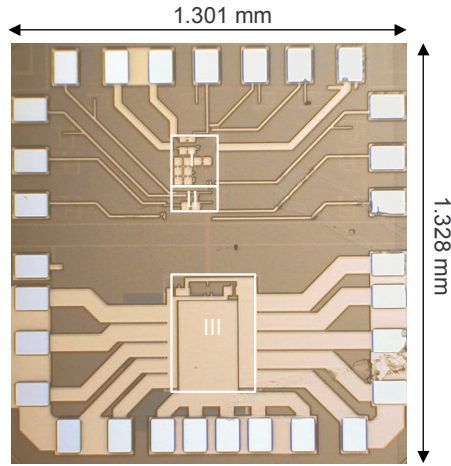


Figure 6.33: Buck converter die micrograph, I compensator (0.0985mm^2), II comparator and carrier signal generator (0.0073mm^2), and III power stage (0.0267mm^2).

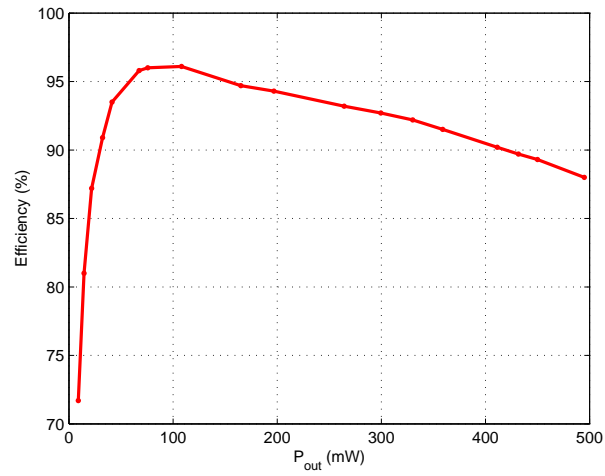


Figure 6.34: Efficiency versus output power.

Table 6.4: Buck converter performance summary

Parameters	[107]	[114]	[115]	This Work
Switching frequency	1 MHz	1 MHz	1 MHz	1 MHz
Maximum output current	600 mA	800 mA	500 mA	550 mA
Maximum power efficiency	97%	96%	90%	96%
Compensator quiescent current	30 μ A	-	-	8.8 μ A
Output ripple voltage	< 10 mV	35 mV	-	< 5 mV
Settling time	7 μ s	-	9 μ s	4.4 μ s
Line Regulation	3 mV/V	9 mV/V	-	0.3 mV/V
Load Regulation	16 mV/A	1.25mV/A	-	4 mV/A
Area	1.32 mm ²	1.82 mm ²	3.04 mm ²	0.1325 mm ²
Technology	0.35 μ m CMOS	0.35 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS

Figure 6.34 shows the measured efficiency versus output power. An efficiency above 87% is achieved from 25 mW to 495 mW, and a maximum efficiency of 96% is obtained at 110 mW. The total quiescent current of the compensator is 8.8 μ A. The efficiency and voltage ripple were measured using the setup shown in Section 5.9.1.

Fig. 6.35(a) shows the load transient measurement setup. The load step is gen-

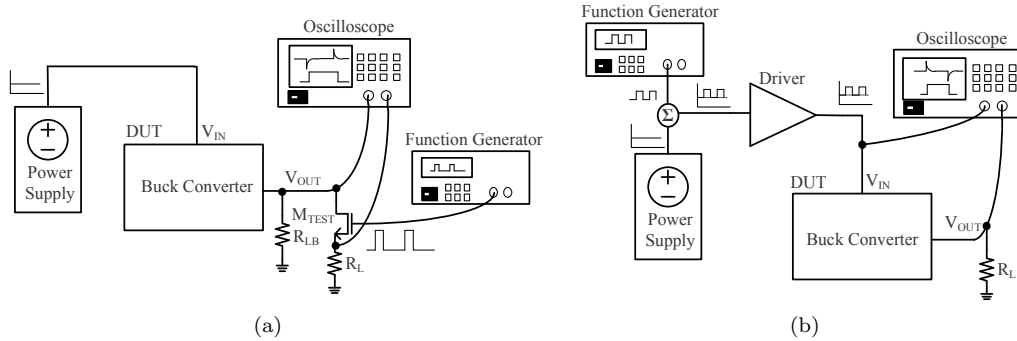


Figure 6.35: Measurement setup for (a) load transient and (b) line transient.

erated by switching the connection between the output voltage V_o and the load resistance R_L using the power FET M_{TEST} . In this test, a square signal at 2 kHz with 20% of duty cycle was applied to the gate of M_1 . Fig. 6.36 shows the load

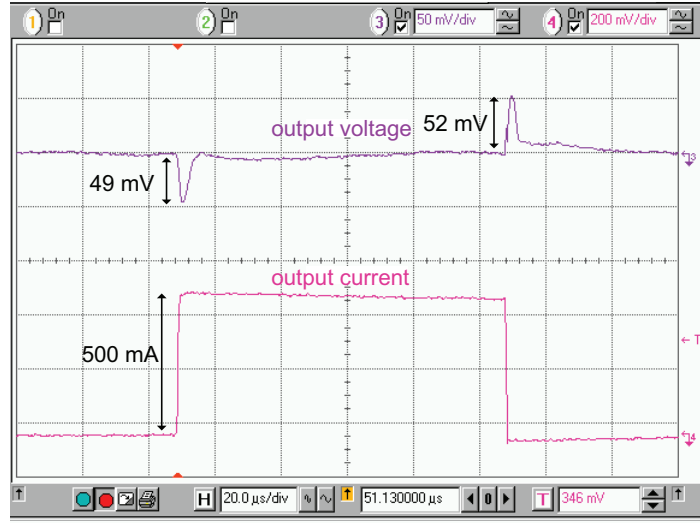


Figure 6.36: Load transient response (x-axis = $20\mu\text{s}/\text{div}$, V_{OUT} y-axis = $50\text{mV}/\text{div}$, and I_L y-axis = $200\text{mV}/\text{div}$).

transient response of the prototype. For this test, a load-current step of 500 mA was applied, and R_L was chosen to be $1\ \Omega$. In Figure 6.36, the voltage dip and voltage surge were 49 mV and 52 mV, respectively. The system settled in the worst case within $4.4\ \mu\text{s}$ for an error of 2%. Good load regulation is achieved because of the high DC loop gain ($> 90\ \text{dB}$ from simulations) and with careful PCB layout.

Fig. 6.35(b) shows the line transient measurement setup. The line transient test was performed with a square signal of $1\ V_{pp}$ at 2 kHz superimposed on a DC level of 1.8 V. A driver between the waveform generator and the V_{IN} pin of the buck converter provides the input current required by the converter. Fig. 6.37 shows the line transient response of the system. In this test, a voltage step at V_{IN} from 1.8 V to 2.8 V and vice versa was applied. From Figure 6.37, the voltage dip and surge were both 37 mV. High line regulation performance is achieved because of the high DC loop gain.

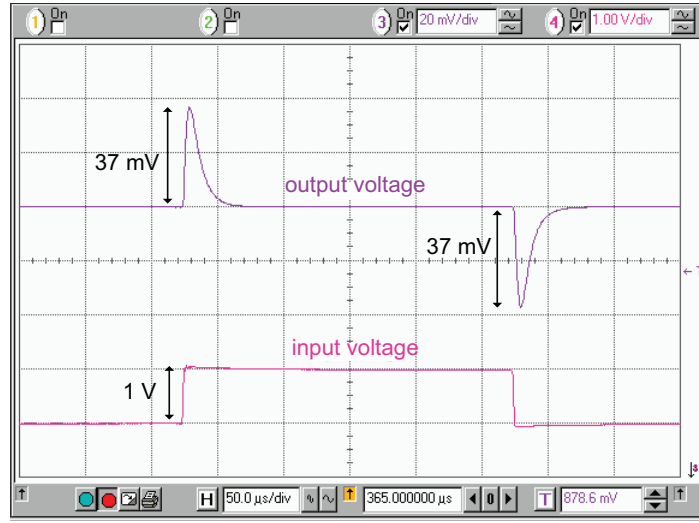


Figure 6.37: Line transient response (x-axis = $50\mu\text{s}/\text{div}$, V_{OUT} y-axis = $20\text{mV}/\text{div}$, and V_{IN} y-axis = $1\text{V}/\text{div}$).

6.5 Conclusion

1. A fully-integrated buck converter was presented. The two-phase converter structure allows 50% reduction of the output current ripple. The proposed converter delivers up to 400 mA at 1 V from a single 1.8 V voltage supply and reaches a maximum power efficiency of 53%. Efficiency can be improved with an enhanced inductor quality factor; for instance, an inductor with $Q_L = 8$ would yield an efficiency of 60% at 200 mA.
2. In addition, the design, implementation, and testing of a 3-switch dual-output buck voltage regulator was presented. A proof-of-concept IC prototype of the voltage regulator was fabricated in $0.5\mu\text{m}$ CMOS technology. The experimental results show consistency with theoretical calculations. It has been demonstrated that the implementation of a dual-output buck voltage regulator can be feasible, reliable, cheap, and versatile. Specifically, the voltage condition

$V_{OUT1} \geq V_{OUT2}$ must be satisfied to properly operate the converter, but the best efficiency and transient performance is obtained when the current condition of $I_{OUT1} \geq I_{OUT2}$ is met. The proposed dual output converter achieves efficiency and maximum output-current levels competitive with state-of-the-art and does so using less static power and silicon area than previous solutions [99]-[100].

3. Finally, the design, implementation, and experimental results of a compact compensator that combines Gm-RC and Active-RC techniques to emulate the conventional Type-III compensation was presented. The prototype reduces the compensator's area by more than 45%, and the total active chip area by approximately 15% when compared with a similar design implemented with the conventional Type-III compensation scheme. The prototype shows good line/load regulation due to high DC loop gain and careful layout. In addition, high efficiency is achieved over a wide output power range. The proposed buck converter operates at 1 MHz of switching frequency and provides a maximum output current of 550 mA.

7. INTRODUCTION TO CLASS-D AUDIO AMPLIFIERS

7.1 Introduction

Class-D audio amplifiers have become very popular due to their inherent high efficiency when compared to other types of audio amplifiers. This feature helps to minimize the heat dissipation in high power applications and to extend the battery life of portable products. They can be found in systems such as: MP3 players, cellular phones, laptops, televisions, home theater systems, cars, and hearing aids.

This section introduces the basics of class-D audio amplifiers and their principles of operation. Moreover, the main close loop class-D audio amplifier topologies and performance metrics are presented. Practical design considerations for class-D audio amplifiers are also provided.

7.2 Types of Audio Amplifiers

The purpose of an audio amplifier is to amplify the low power input audio signal and drive a loudspeaker. Ideally, the amplifier must achieve low distortion and high efficiency over the entire audio frequency range (i.e., 20 Hz to 20 kHz). Before discussing class-D audio amplifiers in detail, the most common audio amplifiers will be introduced.

7.2.1 *Class-A*

In class-A amplifiers, the current continuously flows through the output devices and as a result, it achieves the best linearity performance when compared with the other types of amplifiers. Nevertheless, its maximum theoretical efficiency is only 25%.

7.2.2 *Class-B*

In this topology, the current flows half of the period in each output device and as a consequence, it can achieve a maximum theoretical efficiency of 78.5%. However, it has inferior linearity performance than class-A amplifiers due to the crossover distortion caused when the transistors are transitioning from on and off states.

7.2.3 *Class-AB*

A class-AB amplifier is a combination of class-A and class-B amplifiers. In this topology, both output devices conduct at the same time near the crossover region; thereby eliminating the crossover distortion of class-B amplifiers. Its efficiency performance is similar to a class-B amplifier.

7.2.4 *Class-D*

In class-D amplifiers, the output is continuously switching between the rails at a frequency much higher than the audio signal. This topology can achieve a theoretical maximum efficiency of 100%, but its distortion is inherently high.

7.2.5 *Class-G*

This type of amplifier saves quiescent power by switching between multiple supplies depending on the audio signal level. In an implementation with two supply voltages, the amplifier is powered by a lower supply voltage (V_{DDL}) when the output signal level is below V_{DDL} , and by a higher supply voltage (V_{DDH}) when the output signal level is above V_{DDL} . This results in an efficiency improvement at small output signal levels. A challenge in this topology is to minimize the distortion when switching between supply voltages.

7.3 Class-D Audio Amplifiers

The main advantage of class-D audio amplifiers is their inherent high efficiency over other types of audio amplifiers as mentioned in the previous section. Class-D audio amplifier applications can be classified based on the output power (P_{OUT}) level: (1) low power ($P_{OUT} < 5$ W) and (2) high power (80 W $< P_{OUT} < 1400$ W) [116]. Low power applications include: cellular phones, MP3 players, portable video games, hearing aids, notebooks/netbook computers, etc. These applications are mostly portable and as a result, high efficiency is required to extend battery life [116]. High power applications include: home audio, automotive audio, theaters, etc. Reducing heat dissipation in these type of products is critical to decrease the size of the heatsink and obtain a smaller and more cost effective product [116]. In this dissertation, the emphasis is on low power applications.

Class-D audio amplifier architectures are classified under two categories: open loop and closed loop. Both types of architectures will be described in the following sub-sections.

7.3.1 Open Loop Class-D Audio Amplifier

7.3.1.1 Single-Ended Architecture

Figure 7.1 shows the open loop single-ended class-D audio amplifier architecture. It consists of a carrier signal generator (typically a triangular or sawtooth waveform), a comparator, an output stage, and an output filter. This system operates as follows: The low-frequency audio signal is compared with the high frequency carrier signal to generate the PWM signal with a duty cycle proportional to the average audio signal. The PWM signal controls the power stage, which provides the necessary power to drive the loudspeaker. Finally, a low pass filter, which must have flat frequency response over the audio band (i.e., 20 Hz - 20 kHz), is used to remove the

high frequency components of the PWM signal and recover the low-frequency audio signal.

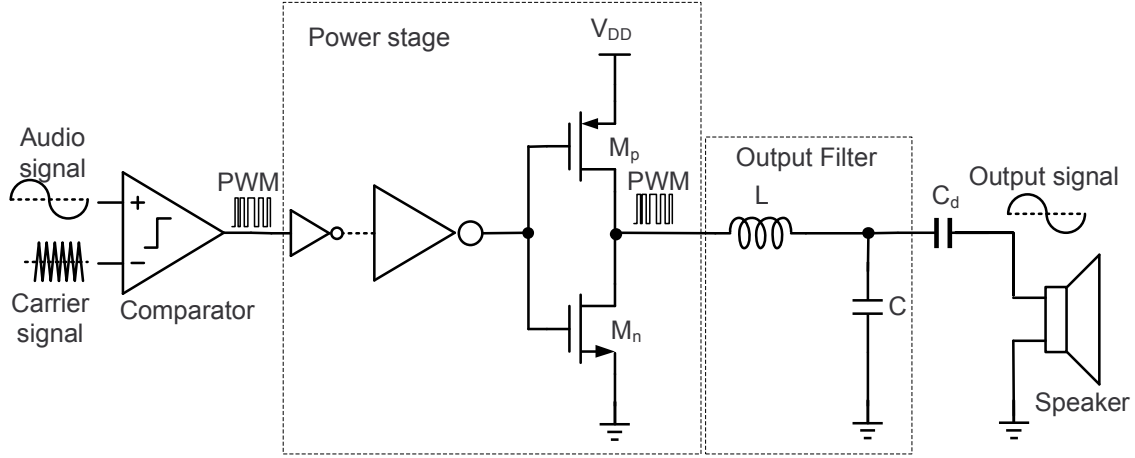


Figure 7.1: Single-ended open loop class-D audio amplifier architecture.

This architecture requires a well regulated supply voltage because its PSRR is very poor within the audio band [117]. In addition, total harmonic distortion (THD) and noise performance may suffer because there is no error correction (e.g., feedback) [118]. This topology can be powered from a single supply voltage (V_{DD}) and ground as the negative supply voltage (V_{SS}). Nevertheless, a decoupling capacitor (C_d) should be placed between the loudspeaker and amplifier to avoid any potential damage caused by the DC bias component (i.e., $V_{DD}/2$) to the speaker [119].

The single-ended class-D audio amplifier has the same building blocks as the synchronous buck converter. However, the main differences between both circuits are the following:

- The reference signal in a synchronous voltage converter is a DC voltage, while in

the class-D audio amplifier, the reference is the audio signal. Hence, the duty cycle in the synchronous buck converter is fixed while in the class-D audio amplifier, it is continuously changing, but on average, it is 50% [120].

- Total harmonic distortion is a very important performance metric in the class-D audio amplifier, while in a synchronous buck converter it is not.
- A synchronous buck converter only sources current to the load, while a class-D audio amplifier can source or sink current to the load [120].
- The R_{on} of the power transistors are optimized differently for efficiency purposes in synchronous buck converters when compared to class-D audio amplifiers. In a synchronous buck converter, the power transistors are optimized such that $R_{on,p} < R_{on,n}$ for large duty cycles, and $R_{on,n} < R_{on,p}$ for low duty cycle (see Section 5 for details). In the case of the class-D audio amplifier, since the average duty cycle is 0.5, $R_{on,n} = R_{on,p}$ [120].

Figure 7.2 shows a suitable block diagram to implement a closed loop synchronous buck converter or class-D audio amplifier in Simulink. The output filter $F(s)$ and compensator $H(s)$ transfer functions can be implemented with the *Transfer Fcn* block in Simulink. The comparator can be implemented with the *Sum* and *Relay* blocks, and the carrier signal generator with the *Repeating Sequence* block. The power stage can also be implemented with the *Relay* block. The reference voltage in the synchronous buck converter and class-D audio amplifier can be implemented with the *Constant* and *Sine Wave* blocks, respectively. Also, notice that in many class-D audio amplifiers, the feedback is taken from the v_{sw} node instead of the v_{out} node in the buck converter.

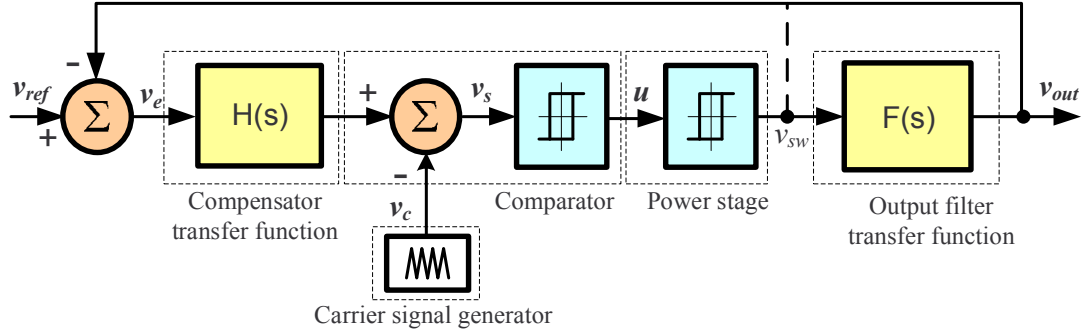


Figure 7.2: System block diagram for the synchronous buck converter or class-D audio amplifier in closed loop.

7.3.1.2 Bridge-Tied Load Architecture

Figure 7.3 shows the differential open loop class-D audio amplifier, also known as bridge-tied load (BTL). The output stage is also known as a H-bridge. In this architecture, the loudspeaker is driven by signals with an opposite phase in each side and as a result, the differential voltage across the loudspeaker is doubled and the output power is quadrupled when compared with the single-ended topology. Another advantage of BTL is the inherent cancellation of even harmonics, which improves linearity performance. However, these benefits come at the expense of increasing the area and cost since this architecture requires twice the number of output stages and inductors [117]. In some cases, twice the amount of comparators and carrier signal generators are also required, but their areas are typically negligible when compared with the occupied area by the output stage and output filter.

BTL architectures typically control the PWM signals that drive the power transistors in the H-bridge using two-level modulation also known as AD modulation or three-level modulation also known as BD modulation. Figure 7.4 (a) shows how the PWM signals are controlled in two-level modulation. Notice that PWM+ is

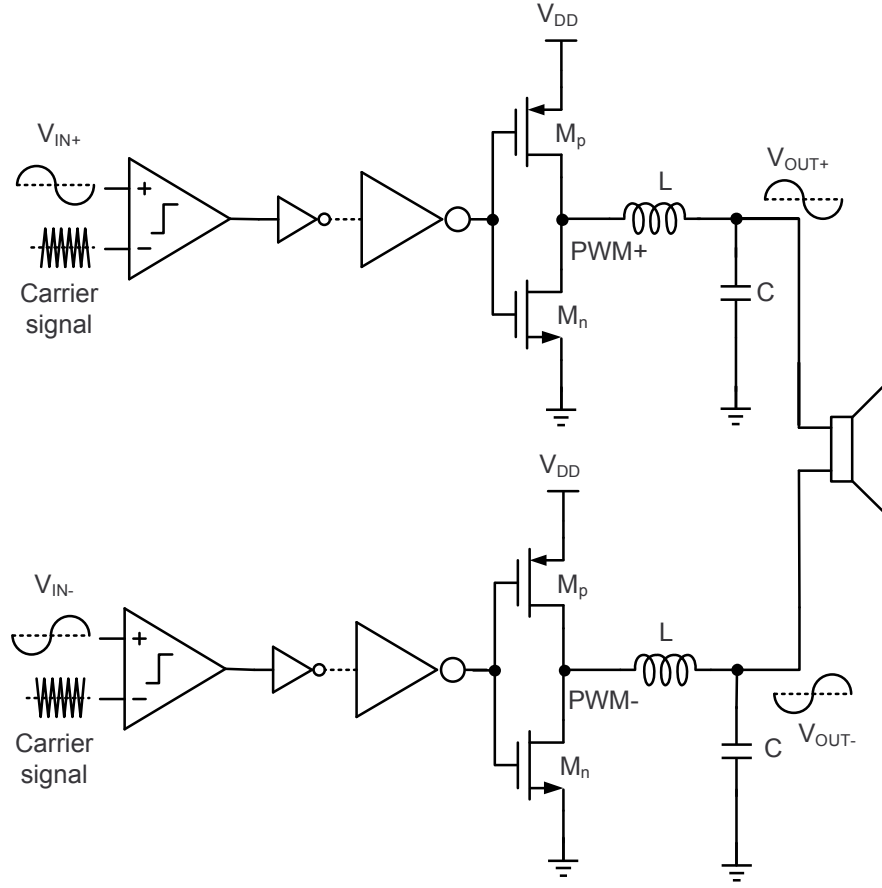


Figure 7.3: Differential open loop class-D audio amplifier architecture.

the inverse of PWM-. This can be obtained with the implementation shown in Figure 7.3 where the carrier signals are 180° out of phase. A class-D audio amplifier implemented with two-level modulation has no significant common mode voltage at the output [121] and the duty cycle of the PWM signal is 50% in the absence of input signal [21]. Figure 7.4 (b) shows the generation of three-level modulation. From Figure 7.4, it can be seen that PWM+ and PWM- are in phase and that the differential PWM signal (i.e., PWM+ - PWM-) has three voltage levels. A class-D audio amplifier implemented with three-level modulation has no output pulses in the

absence of an input signal [21].

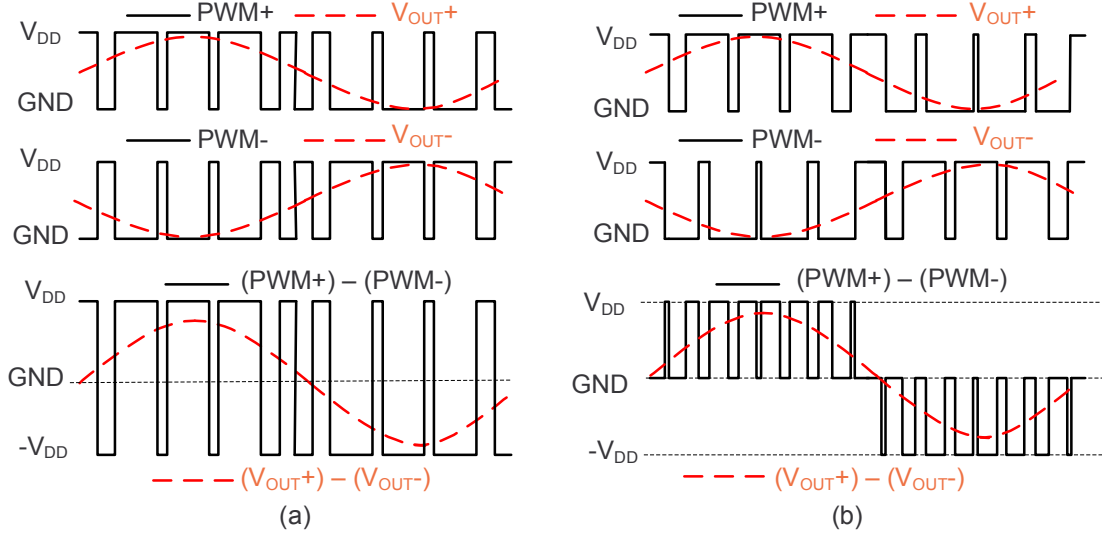


Figure 7.4: (a) Two-level (b) three-level modulation signals.

7.3.2 Closed Loop Architecture

In this section, class-D audio amplifier topologies that employ feedback to improve PSRR and linearity are discussed.

7.3.2.1 Closed Loop Pulse Width Modulation Topology

Figure 7.5 shows a first order closed loop PWM class-D audio amplifier. The loop transfer function of this system is given by:

$$H(s) = -\frac{G_{mod}}{R_1 C_1} \cdot \frac{1}{1 + \frac{1}{A(s)} \cdot \left(1 + \frac{2}{R_1 C_1}\right)} \quad (7.1)$$

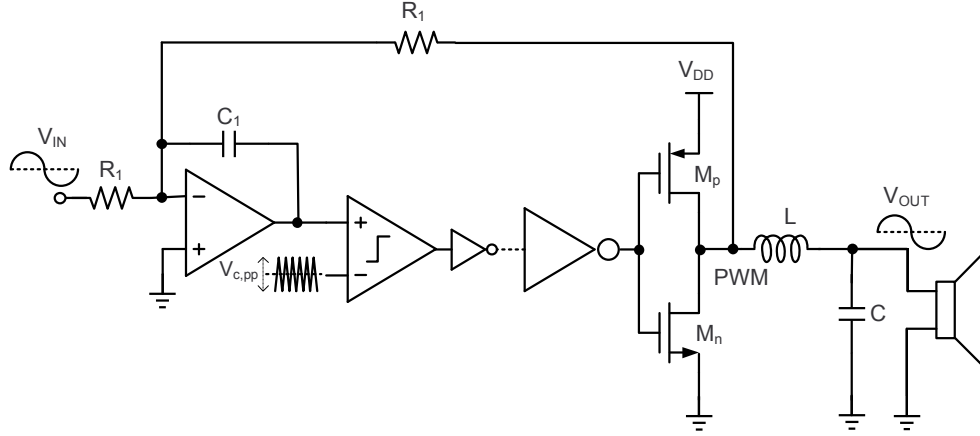


Figure 7.5: Single-ended PWM closed loop class-D audio amplifier architecture.

where G_{mod} is the supply voltage (V_{DD}) over the peak-to-peak amplitude of the carrier signal ($V_{c,pp}$). For example, when $V_{DD} = 5$ V and $V_{c,pp} = 2.5$ V, $G_{mod} = 2$ V/V. Parameter $A(s)$ represents the amplifier transfer function. Assuming $A(s) = A_o/(1 + s/\omega_{po})$ and large DC amplifier gain (A_o), (7.1) can be expanded and simplified to:

$$H(s) = -\frac{G_{mod}A_o}{2} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (7.2)$$

where

$$\omega_{p1} = \frac{2}{A_o R_1 C_1}, \quad \omega_{p2} = A_o \omega_{po}$$

The unity gain frequency of the loop is:

$$\omega_u = \frac{G_{mod}}{R_1 C_1} \quad (7.3)$$

7.3.2.2 Closed Loop $\Delta\Sigma$ Topology

Figure 7.6 shows a closed loop $\Delta\Sigma$ class-D audio amplifier architecture. It consists

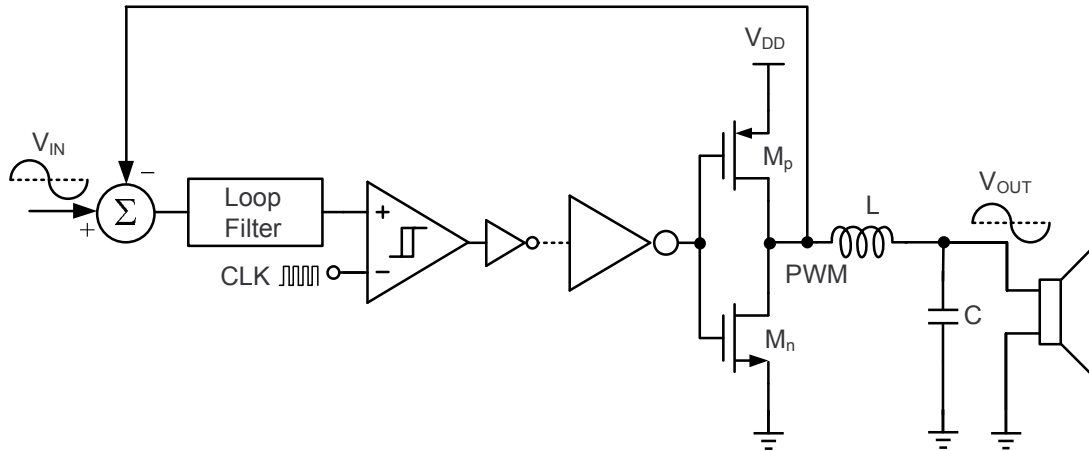


Figure 7.6: Single-ended closed loop $\Delta\Sigma$ class-D audio amplifier architecture.

of a loop filter, single-bit quantizer (comparator), power stage, and output filter. The quantizer (comparator) is 1-bit since it drives the power switches; however, a 1.5 bit topology can be employed in a fully differential architecture with three-level modulation [122]. The $\Delta\Sigma$ architecture provides inherent noise shaping characteristics which minimizes the noise in the audio band, and as a result, improves SNR performance. Moreover, the $\Delta\Sigma$ architecture can potentially achieve better EMI performance than PWM since its high-frequency energy is distributed over a wide frequency range and it is not concentrated over the harmonics of the switching frequency [119].

The typical clock frequencies are between 3 MHz and 6 MHz [119] to avoid efficiency degradation due to an increase in switching losses. Low clock frequency implies low over-sampling ratio (OSR) and as a result, a high order loop filter (e.g., $> 5^{th}$ order) is required to achieve high SNR performance. The loop filter's zeros are typically placed to achieve noise-shaping in the audio-band, while the poles should be carefully placed to avoid instability at high input amplitudes [123]. This high order filter increases the quiescent power consumption and hence, it may be an issue

in low-power applications. In [124], a quantizer with dynamic hysteresis reduces the equivalent switching frequency of the amplifier to decrease switching losses. Dynamic hysteresis also provides stability over a wide range of input amplitudes.

7.3.2.3 Closed Loop Hysteretic Topology

Figure 7.7 shows a typical hysteretic class-D audio amplifier architecture. This

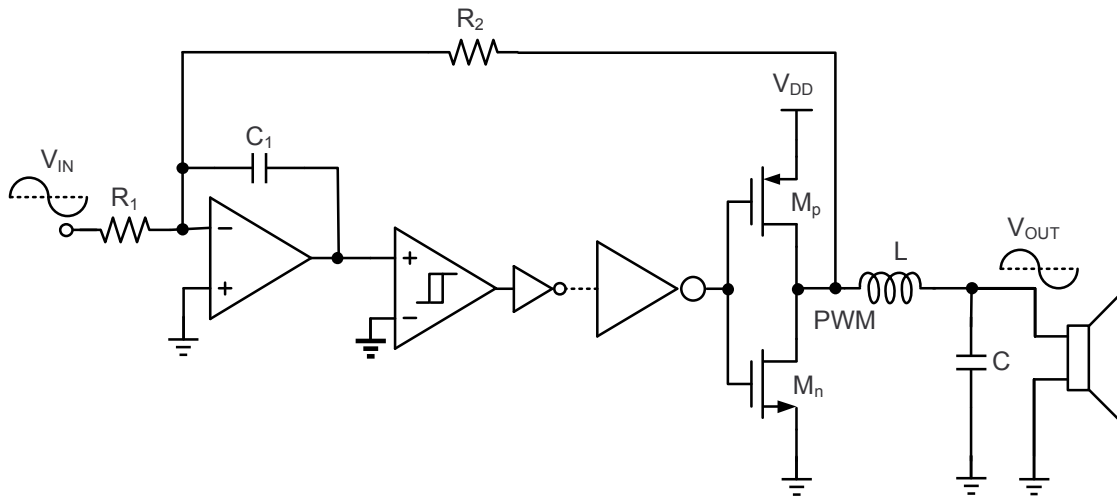


Figure 7.7: Single-ended closed loop hysteretic class-D audio amplifier architecture.

architecture is very simple, and it does not require a carrier signal generator as is the case with PWM topologies or a complicated modulator required by $\Delta\Sigma$ architectures. As a result, hysteretic architectures can save area and quiescent power. The loop switching frequency of this architecture is given by [117]:

$$f_s = \frac{1 - M^2}{4 \cdot h \cdot R_2 C_1} \quad (7.4)$$

where h is the ratio between the hysteresis window of the comparator and supply voltage V_{DD} , and M is the modulation index. A drawback of this architecture is that f_s is not constant, and it varies with the modulation index. This variation in f_s makes synchronization with other switching circuits in the system difficult [119] and complicates electromagnetic interference shielding in electronics equipment. In multi-channel systems, audio intermodulation products are produced by the difference in switching frequencies among channels [117].

7.3.2.4 *Sliding Mode Control*

The power stage of a class-D audio amplifier is a variable structure system (VSS) in nonlinear control theory, and as a result, its controller can be implemented with a nonlinear control method such as sliding mode control. Sliding mode control development started in the 1950s in the Soviet Union and has been applied to systems such as power converters, aircrafts, robotics, etc [125]. Sliding mode provides robustness to parameter variations, rejection to external perturbations, and relatively simple implementations [125].

To the author's knowledge, the first class-D audio amplifier with sliding mode control was proposed in 1998 [126]. Nevertheless, it was not until late in 2000s that the first monolithic class-D audio amplifiers based on sliding mode control were implemented [64]-[66]. These implementations achieve good linearity performance and very low quiescent power consumption, which make them very attractive in portable applications. In the next section, a class-D audio amplifier with integral sliding mode control is proposed to further reduce the quiescent power consumption.

Figure 7.8 shows the block diagram of a class-D audio amplifier with sliding mode control. More details and fundamentals of sliding mode control can be found in Appendix B.

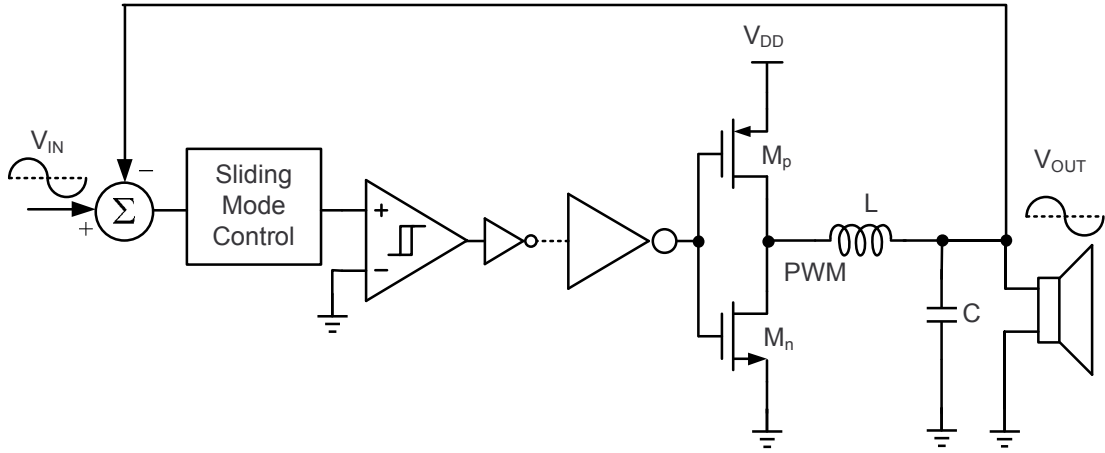


Figure 7.8: Class-D audio amplifier based on sliding mode control block diagram.

7.3.3 Digital Class-D Audio Amplifiers

Analog input class-D audio amplifiers require a digital-to-analog converter (DAC) at their input to convert the digital audio signal to analog as shown in Figure 7.9 (a). A digital input class-D audio shown in Figure 7.9 (b) uses digital PWM to remove the DAC from the system solution. The input $x[n]$ to both systems in Figure 7.9 can be digital data from an MP3 file, CD, DVD, etc. [118]. The $\Sigma\Delta$ stage is necessary to decrease the PWM carrier signal frequency to acceptable values [127]. Digital class-D audio amplifiers are mostly open loop systems as shown in Figure 7.9 (b), and they can achieve good SNR and THD performance at the expense of high clock rates provided a well regulated supply voltage is used [117]. As in analog solutions, a feedback loop can improve PSRR and THD performance [127]. Nevertheless, this requires an analog-to-digital converter to cover the analog output signal to the digital domain, which increases power consumption. Open loop digital class-D audio amplifier can be found in mobile [127] and hearing aid applications [128] to increase

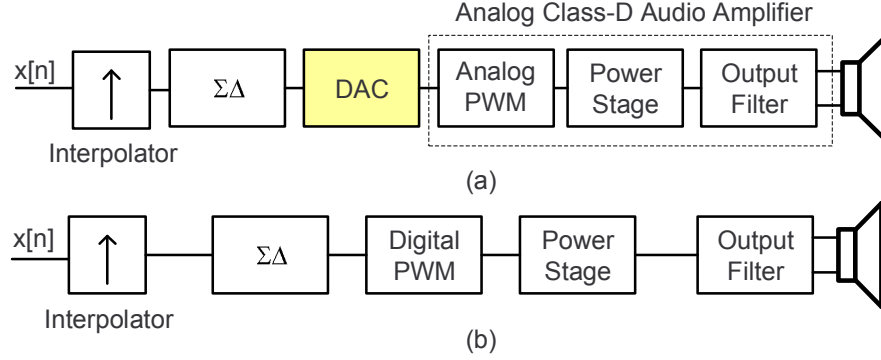


Figure 7.9: Audio system with (a) analog and (b) digital input class-D audio amplifier.

the system's efficiency and hence, extend battery life. Other applications include: television sets and home-theatre systems [117].

7.3.4 Filter-Less Class-D Audio Amplifiers

The main drawback of class-D audio amplifiers is the large occupied board space and high cost of the output filter (i.e., inductor). In low-cost, low-power applications such as audio amplifiers for cellular phones, the price of the output filter could be larger than the amplifier IC [119]. To deal with this issue, class-D audio amplifiers without output filter, also called filter-less class-D audio amplifiers, have been proposed. Figure 7.10 shows a typical filterless class-D audio amplifier implementation that employs BD-modulation to reduce the high frequency energy [117]. In this architecture, the loudspeaker is used as a low pass filter. Figure 7.11 shows a simplified model for the loudspeaker [118], where L_C and R_C are the voice coil inductance and resistance, respectively. The minimum required inductance in a filter-less class-D audio amplifier to achieve good audio efficiency is given by [118]:

$$L_c \geq \frac{R_c}{2\pi \cdot 20kHz} \quad (7.5)$$

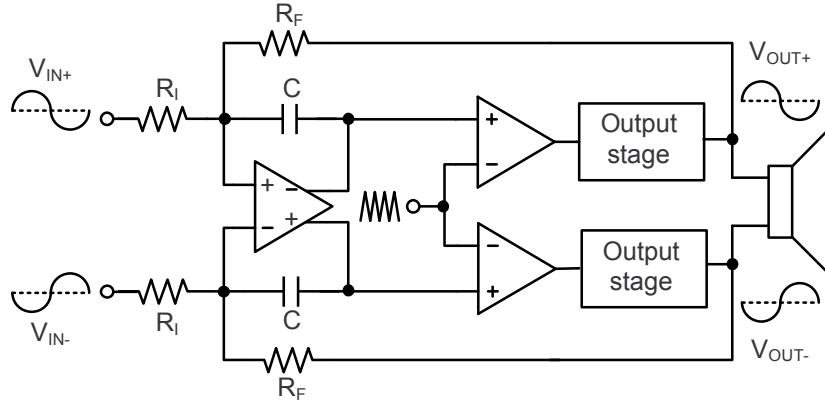


Figure 7.10: Filter-less class-D audio amplifier with BD-modulation.

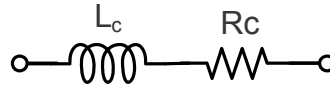


Figure 7.11: Simplified loudspeaker model.

In this architecture, it is recommended to place a highly inductive speaker as close as possible to the amplifier to reduce high frequency power dissipation and EMI [119]. If EMI is of concern, a 2nd order low-pass filter implemented with ferrite beads instead of inductors can be used. The cut-off frequency of this filter is typically between 5 MHz and 10 MHz to attenuate the high frequency components that could cause EMI [129].

7.3.5 Performance Metrics of Class-D Audio Amplifiers

Class-D audio amplifiers specifications include: efficiency, total harmonic distortion (THD), total harmonic distortion plus noise (THD+N), signal-to-noise (SNR), power supply rejection ratio (PSRR), and power supply intermodulation distortion

(PS-IMD) [21], [130]-[133].

Basic class-D audio amplifier characterization requires the following measurement equipment: power supplies, power resistors, multi-meter, oscilloscope, very low distortion signal generator, and audio signal analyzer or spectrum analyzer [21], [130]-[131].

7.3.5.1 Efficiency

Figure 7.12 shows an efficiency measurement setup for class-D audio amplifiers. Resistor R_1 is utilized to measure the power supply current ($I_{DD} = V_{R1}/R_1$) of the

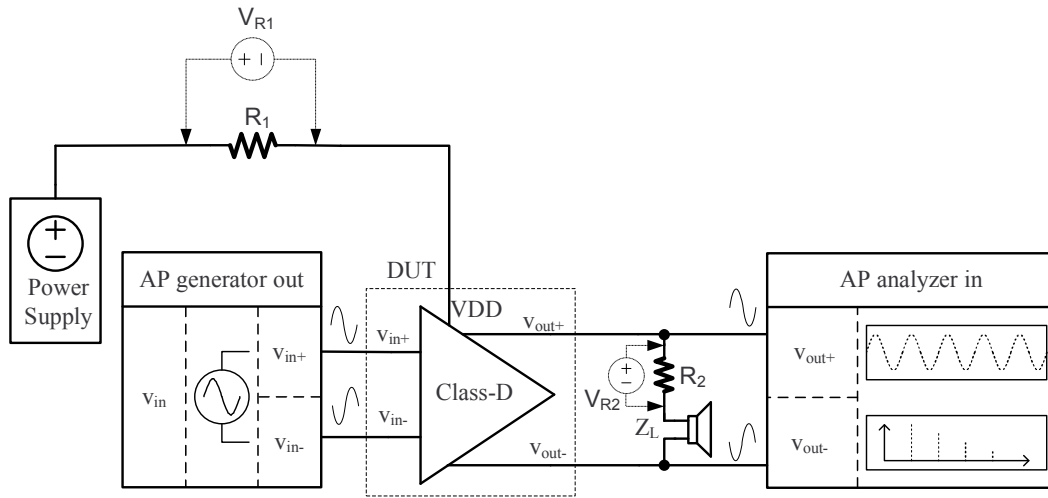


Figure 7.12: Testbench setup for efficiency measurements.

class-D audio amplifier and its value is typically in the range of milli-Ohms (i.e., 100 m Ω) [21], [130]. Resistor R_2 is used to measure the output current ($I_{OUT} = V_{R2}/R_2$) and its value should be smaller (typically 1/10) than Z_L [21]. Resistors R_1 and R_2 are typically power resistors since they need to handle high power dissipation. The

efficiency is typically measured by sweeping the amplitude of a 1 kHz sinusoidal waveform [131], and it can be calculated as:

$$\eta(\%) = \frac{P_{OUT}}{P_{VDD}} = \frac{V_{OUT,RMS} \cdot I_{OUT,RMS}}{V_{DD,AVE} \cdot I_{DD,AVE}} = \frac{V_{OUT,RMS} \cdot \left(\frac{V_{R2,RMS}}{R_2}\right)}{V_{DD,AVE} \cdot \left(\frac{V_{R1,RMS}}{R_1}\right)} \quad (7.6)$$

The output power can be also calculated from the rms voltage measurement on the audio analyzer [131]. The audio analyzer can provide output power readings for an assumed load resistance.

7.3.6 Total Harmonic Distortion

The total harmonic distortion test is performed with a highly linear sinusoidal signal at the input of the system (i.e., audio analyzer outputs), and the output spectrum can be measured with the audio analyzer inputs as shown in Figure 7.13. Ideally, only the fundamental tone of the input signal is present at the output,

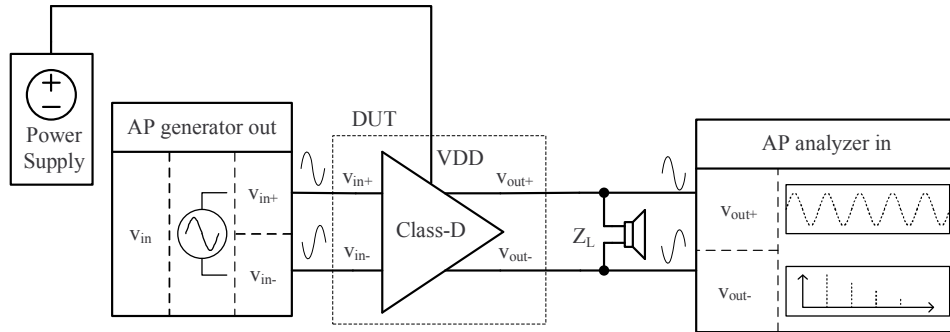


Figure 7.13: Testbench setup for THD, THD+N, and SNR measurements.

but due to the non-linearities of the amplifier, the output waveform consists of the fundamental tone of the input sine wave plus integer multiples (harmonics) of the

input frequency. The percentage (%) of total harmonic distortion in a class-D audio amplifier is given by:

$$THD(\%) = 100 \cdot \left(\frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + \dots + H_k^2}}{H_1} \right) \quad (7.7)$$

and the total harmonic distortion in decibels (dB) can be expressed as:

$$THD(dB) = 20 \log_{10} \left(\frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + \dots + H_k^2}}{H_1} \right) \quad (7.8)$$

where H_1 is the power level of the fundamental frequency, H_k is the power level of the k^{th} harmonic, and k is the maximum harmonic below the upper limit of the audio frequency band (i.e., 20 kHz) [21]. The lower the total harmonic distortion, the better the audio quality.

7.3.7 Total Harmonic Distortion Plus Noise

The total harmonic distortion plus noise (THD+N) test includes the effects of the distortion, noise, and other undesired signals (within the audio band) in one measurement [130]. The total harmonic distortion plus noise can be expressed as [21]:

$$THD + N(\%) = 100 \cdot \left(\frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + \dots + H_k^2 + n^2}}{H_1} \right) \quad (7.9)$$

and

$$THD + N(dB) = 20 \log_{10} \left(\frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + \dots + H_k^2 + n^2}}{H_1} \right) \quad (7.10)$$

when n is the noise voltage level. Both, THD and THD+N measurements are usually reported versus output power and versus frequency [21], [131]. THD and THD+N

versus output power measurements are typically performed with a 1 kHz sinusoidal signal [131].

7.3.8 Signal-to-Noise Ratio

The signal-to-noise ratio is defined as the maximum output voltage compared to the integrated noise floor over the audio bandwidth. The integrated noise floor can be measured by connecting the inputs of the class-D audio amplifier in Figure 7.13 to AC ground. The SNR can be calculated as:

$$SNR(dB) = 20 \log_{10} \left(\frac{V_{RMS,OUT}}{V_{RMS,N}} \right) \quad (7.11)$$

where $V_{RMS,N}$ and $V_{RMS,OUT}$ are the integrated RMS noise floor and maximum RMS output voltage.

7.3.9 Power Supply Rejection Ratio and Power Supply Intermodulation Distortion

Figure 7.14 shows an test measurement setup for the PSRR. This test is performed

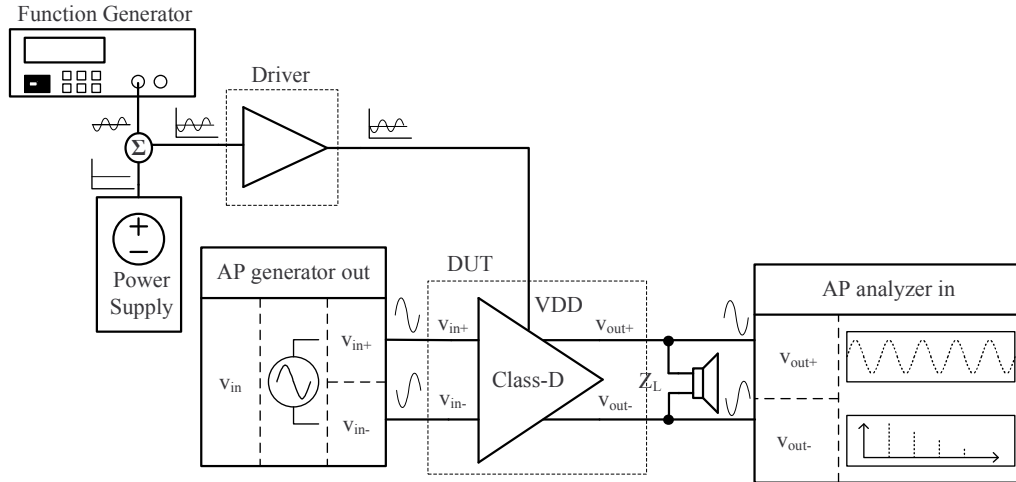


Figure 7.14: Testbench for PSRR and PS-IMD measurements.

with a sinusoidal signal (typically 100 mV amplitude) superimposed on a DC voltage level of V_{DD} while the inputs of the class-D audio amplifier are AC grounded. The driver is added between the waveform generator, and the V_{DD} of the class-D audio amplifier to provide the required current. This driver is particularly necessary since a waveform generator is not capable of providing currents above a few milliamps. The PSRR can be expressed as:

$$PSRR(dB) = 20\log_{10}\left(\frac{V_{OUT}}{V_{DD}}\right) \quad (7.12)$$

where V_{OUT} is the output voltage, and V_{DD} is the AC magnitude at the output of the driver.

The power supply intermodulation distortion test can be done using the same test measurement shown in Figure 7.14, but the inputs of the class-D audio amplifier are connected to a sinusoidal signal instead of AC ground [132]-[134]. More details about this test will be provided in Section 8.4.

7.3.10 Practical Considerations

As mentioned previously in this section, class-D audio amplifiers and buck converters have abundant similarities and possess the same building blocks. Hence, the practical design considerations provided in Section 5 for the comparator, carrier signal generator, output power stage, layout, printed circuit board, etc. apply for class-D audio amplifiers as well [21].

8. A LOW QUIESCENT POWER HIGH-PSRR CLASS-D AUDIO AMPLIFIER*

8.1 Introduction

Portable electronics' demands for low power consumption to extend battery life and reduce heat dissipation mandate efficient, high-performance audio amplifiers. Class D amplifiers' (CDAs') high efficiency makes them particularly attractive for portable applications. However, their inherently high distortion and poor power supply rejection ratio (PSRR) relative to linear amplifiers (e.g., class AB) often preclude their use in portable applications. To overcome these challenges, the complexity and power consumption of the CDAs are typically increased. Thus, the main challenge is to design a class-D audio amplifier that has high efficiency and good linearity while improving the PSRR and minimizing the controller's power consumption.

Class-D amplifiers comprise several main topologies. Architectures based on pulse-width modulation (PWM), cf. Figure 8.1, are perhaps the most popular and have been used as controllers for the class-D amplifiers for many years. Open-loop architectures require a precise carrier signal to achieve low distortion [135]. Closed-loop architectures do not require as precise carrier because the CDA loop gain suppresses carrier distortion [136]. However, closed-loop architectures nonetheless need a carrier signal generator block and these architectures often must consume considerable power to achieve low distortion [132]. Alternatively, some CDAs comprise a single-bit $\Delta\Sigma$ modulator as shown in Figure 8.2, but ensuring stability over all modulation indices mandates high controller power [124]. Multi-bit quantizers

*Reprinted with permission from "A Low-Power High-PSRR Clock-Free Current-Controlled Class-D Audio Amplifier," by J. Torres et al., *IEEE J. Solid State Circuits*, vol. 46, issue 7, pp. 1553-1561, July 2011, © 2011 by IEEE.

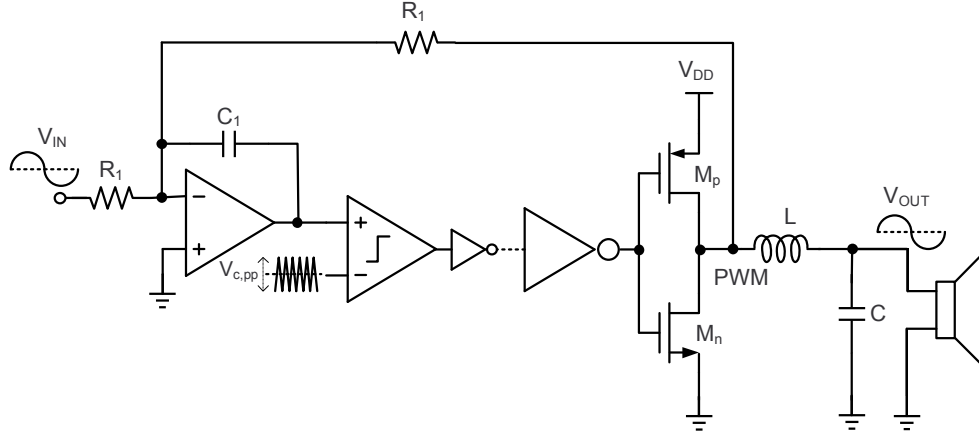


Figure 8.1: Conventional PWM class-D audio amplifier.

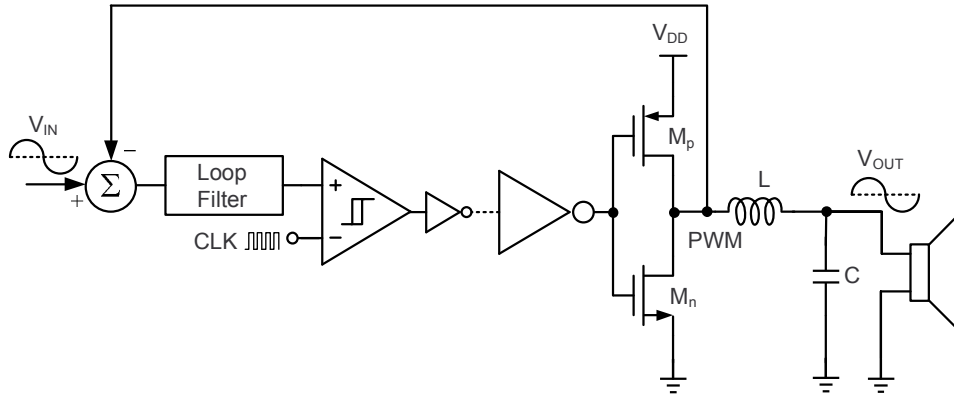


Figure 8.2: Single-bit $\Delta\Sigma$ class-D audio amplifier architecture.

could improve $\Delta\Sigma$ modulators stability, but nevertheless entail high quiescent power and considerable complexity. In [137], a self-oscillating CDA as shown in Figure 8.3 with low distortion is presented; however, the modulator consumes a considerable amount of power. Architectures using variable structure control (VSC) based on sliding mode control (SMC) as shown in Figure 8.4 can decrease the power consumption, achieve low distortion, and reduce the complexity of the system [64]-[66]. Still,

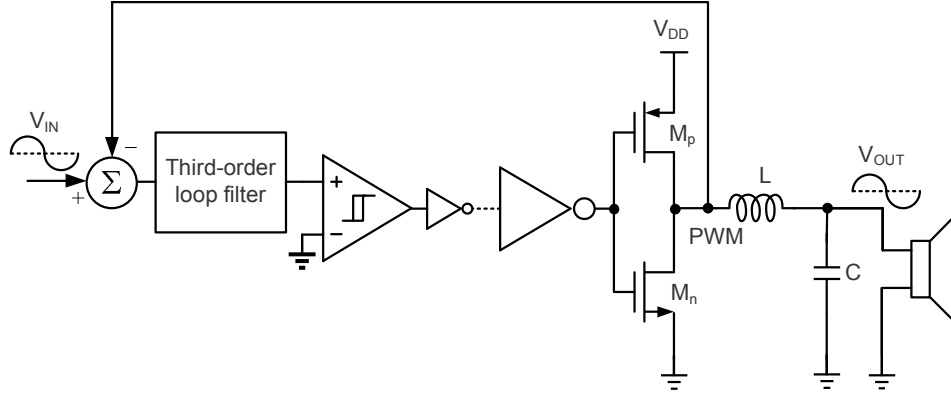


Figure 8.3: Self-oscillating class-D audio amplifier architecture.

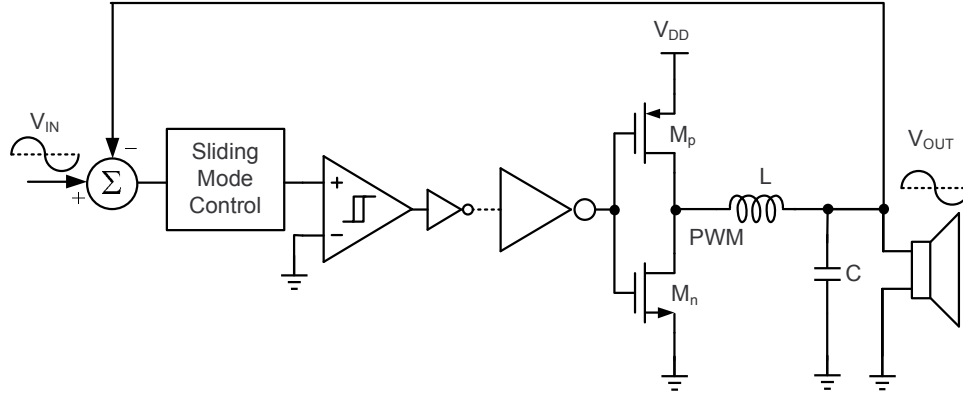


Figure 8.4: Sliding mode control class-D audio amplifier architecture.

this approach is prone to high-frequency noise, as it requires a differentiator in the feedback loop. Also, this topology has a limited power supply rejection ratio (PSRR) in the audio band because the differentiator's low-frequency attenuation reduces the loop gain. To overcome this limitation, we propose a CDA with integral sliding mode control (ISMC) [63] to increase the low-frequency loop gain above that in [64]-[66] and to keep the controller power consumption low.

This section presents a clock-free current-controlled CDA using integral sliding

mode control. The proposed CDA provides the low distortion and high efficiency benefits of state-of-the-art CDAs, but consumes at least 30% less controller power. Additionally, the proposed design improves the PSRR mainly due to good matching. Also, improvement of PSRR is obtained by higher loop gain within the audio band when compared with [64]-[66].

This section is organized as follows: Section 8.2 discusses the design of the proposed architecture. The circuit implementation is described in Section 8.3. Section 8.4 presents the experimental results, and Section 8.5 provides the conclusions.

8.2 Design of the Proposed Class-D Architecture

Figure 8.5 shows the block diagram of the proposed architecture. This topology consists of two feedback loops and four main building blocks. The outer voltage loop

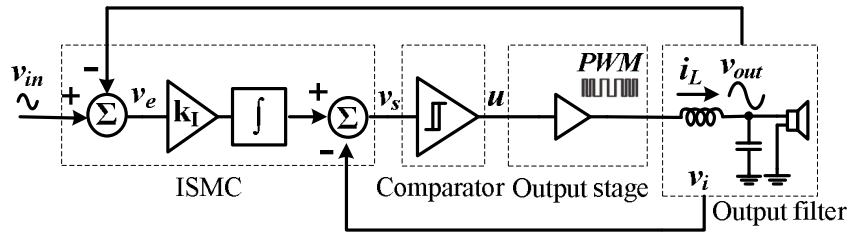


Figure 8.5: Block diagram of the proposed class-D amplifier.

minimizes the voltage error between the input and output audio signals, and the inner current loop contains information proportional to the inductor current which is necessary to implement the controller, as will be explained later in this section. The building blocks are the integral sliding mode controller, a hysteretic comparator, an output stage, and an off-chip low-pass filter (LPF). The ISMC processes the necessary information to generate the binary modulated signal. The hysteretic

comparator obviates the carrier signal generator that would have been required in conventional architectures based on PWM [132]. The output stage provides the required current-drive capability for an 8- Ω loudspeaker, and the output filter recovers the audio signal. This architecture can achieve good linearity, high efficiency, and high power supply rejection while consuming low quiescent power and small silicon area. However, its switching frequency is variable and as a result, EMI is unpredictable and synchronization with other switching circuits in the system is difficult. The audio amplifier implements a tracking system governed by a control law, defined with the switching function [138]-[140] given by

$$s(v_e, v_i) = k_I \int v_e(t) dt - v_i(t), \quad (8.1)$$

where k_I is an integration constant whose value ensures stability and fast transient response, $v_e(t)$ is the voltage error function defined as

$$v_e(t) = v_{in}(t) - v_{out}(t), \quad (8.2)$$

and $v_i(t)$ is a sensed voltage proportional to the inductor current $i_L(t)$.

The ISMC retains all the properties of variable structure control (VSC) with sliding-mode operation such as simple design, stability, robustness, and good transient response. Moreover, the ISMC forces the system to operate with sliding mode under any initial condition [63]. This property guarantees robust system operation from any starting point. The ISMC's integrator nulls the steady-state voltage error, and the closed-loop dynamics reduce high-frequency noise [138]. Furthermore, sensing the current across the output inductor improves the dynamic response of the amplifier [138], [141].

The system can be proven to be asymptotically stable with the equivalent control method analysis [63], as derived in the Appendix C. This method consists of determining the dynamics of the system on the switching surface, i.e. $s(v_e, v_i) = 0$. The sliding-equilibrium point of the proposed architecture is a stable focus because the eigenvalues of the system are complex with negative real part. Moreover, the final value theorem (FVT) shows that the steady-state response of the equivalent control model tracks the input signal [66].

8.3 Building Blocks Implementation

8.3.1 Integral Sliding Mode Controller

Figure 8.6 shows the schematic of the implemented CDA. The blocks marked as I, II, III and IV are the ISMC, comparator, output power stage, and LPF, respectively.

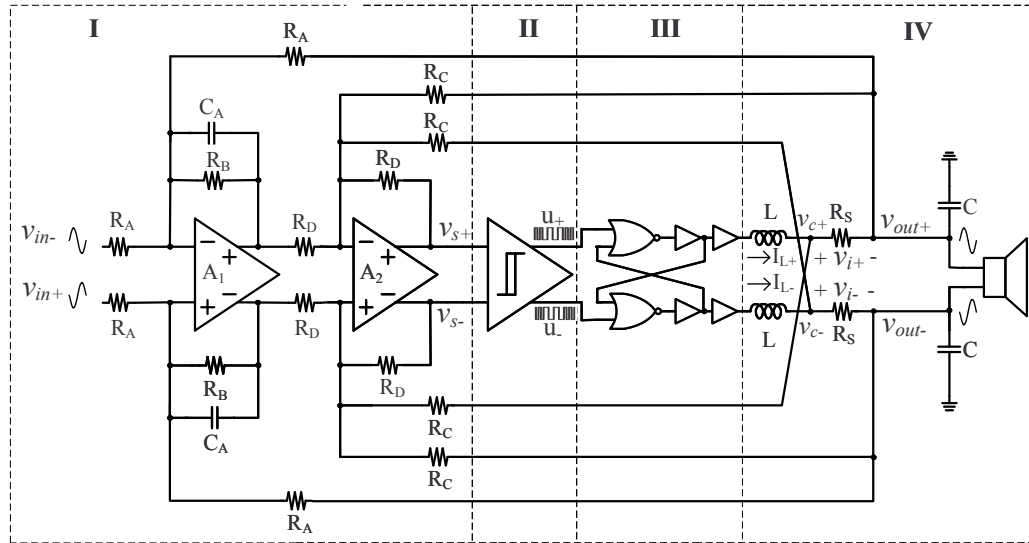


Figure 8.6: Proposed class-D audio amplifier implementation, I ISMC, II comparator, III output power stage, IV LPF.

Examining the node $v_{s\pm}(t)$ one obtains the switching function implemented as

$$s(v_e, v_i) = k_I \int [v_{in\pm}(t) - v_{out\mp}(t)] dt - v_i(t), \quad (8.3)$$

where

$$\begin{aligned} v_i(t) &= k_s \cdot R_s \cdot i_L(t) \\ &= k_s [v_{c\pm}(t) - v_{out\pm}(t)] \\ &= k_s [v_{c\pm}(t) + v_{out\mp}(t)] \end{aligned} \quad (8.4)$$

represents the voltage proportional to the current $i_L(t)$ across the inductor and $k_s = R_D/R_C$. Equations (8.3) and (8.4) describe the implemented controller circuit. The proposed CDA uses two external precision resistors (R_s) in series with the filter inductor to sense the inductor current and to feed it back to the controller. The value of these resistors was chosen high enough to sense the voltage across the resistor but sufficiently small to minimize its impact on the power efficiency of the system. Figure 8.7 shows the tradeoff between the R_s value and the efficiency of the CDA when $V_{in} = 2 V_{pp}$; the smaller R_s , the higher the efficiency. However, an excessively small value of R_s could be comparable to parasitic board/package resistances, reducing measurement accuracy. We choose $R_s = 100 \text{ m}\Omega$ to achieve both good accuracy and high efficiency, we choose $k_s = 10$ to have a voltage $v_i(t)$ directly proportional to $i_L(t)$. Note that other current sensing techniques could be employed in the ISMC architecture to improve efficiency and/or to reduce the external component count [57].

A fully differential amplifier (A_2) senses the inductor current using cross con-

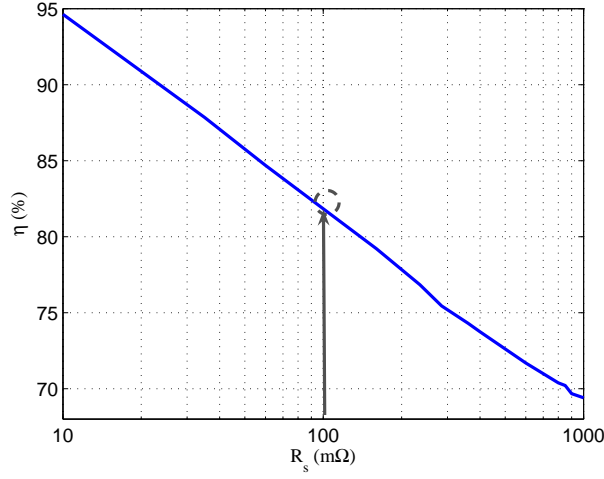


Figure 8.7: Efficiency versus R_s for $V_{in} = 2 V_{pp}$.

nected $v_{c\pm}(t)$ nodes. The THD of a closed loop amplifier can be written as [21], [64]:

$$THD \approx \sqrt{\left(\frac{HD_2}{(1 + \beta A)^2}\right)^2 + \left(\frac{HD_3}{(1 + \beta A)^3}\right)^2 + \dots + \left(\frac{HD_N}{(1 + \beta A)^N}\right)^2} \quad (8.5)$$

where HD_N is the N^{th} harmonic distortion component of the amplifier in open loop and βA is the loop gain of the amplifier. As can be seen from (8.5), the larger the loop gain, the better the THD. Hence, good THD mandates sufficiently high amplifier gain bandwidth product (GBW). Figure 8.8 depicts the trade-off between CDA's THD and the amplifier GBW. For $GBW < 1$ MHz, the THD performance is considerably degraded, and > 10 MHz there is no considerable THD enhancement. Thus, we choose $GBW = 10$ MHz to achieve high THD and minimize power consumption. The integrator (A_1), on the other hand, only needs to process low-frequency audio signals (not the high-frequency switching signal); hence $GBW = 600$ kHz suffices for the (fully differential) integrator. The lossy integrator resistors R_B limit the low-frequency gain to prevent the amplifier from saturating [124].

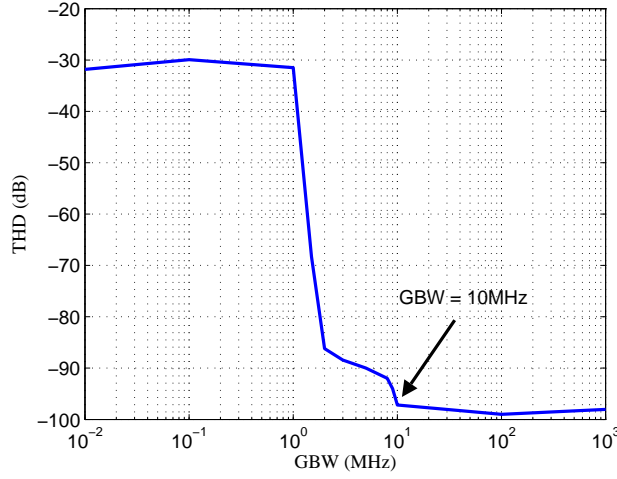


Figure 8.8: THD versus GBW of the current sensing amplifier (A_2).

Both the lossy integrator (A_1) and current sense (A_2) amplifiers are two-stage-Miller compensated [78] and consume $35 \mu\text{A}$ and $90 \mu\text{A}$ of static current, respectively. Figure 8.9 shows the transistor-level implementation of the amplifiers. The DC open-loop gain (A_o), dominant pole (ω_{p1}), and GBW of this amplifiers can be expressed as:

$$A_o = \frac{g_{m1}g_{m3}}{(g_{ds1} + g_{ds2}) \cdot (g_{ds3} + g_{ds4})}, \quad \omega_{p1} = \frac{(g_{ds1} + g_{ds2}) \cdot (g_{ds3} + g_{ds4})}{g_{m3}C_c}, \quad (8.6)$$

$$GBW = \frac{g_{m1}}{C_c}$$

where g_{mi} and g_{dsi} (for $i = 1, 2, 3, 4$) represent the transconductances and conductances of the transistors, respectively. Parameter C_c is the Miller compensation capacitor, and zero $\omega_{z1} = 1/(R_c C_c)$ is used to increase the phase margin. Amplifier (A_1) has a DC open-loop gain of 68 dB and a phase margin of 59° and amplifier (A_2) has a DC open-loop gain of 62 dB and a phase margin of 45° .

The lossy-integrator has $k_I = 1/R_A C_A = 1.78 \cdot 10^5$ for fast transient response [65],

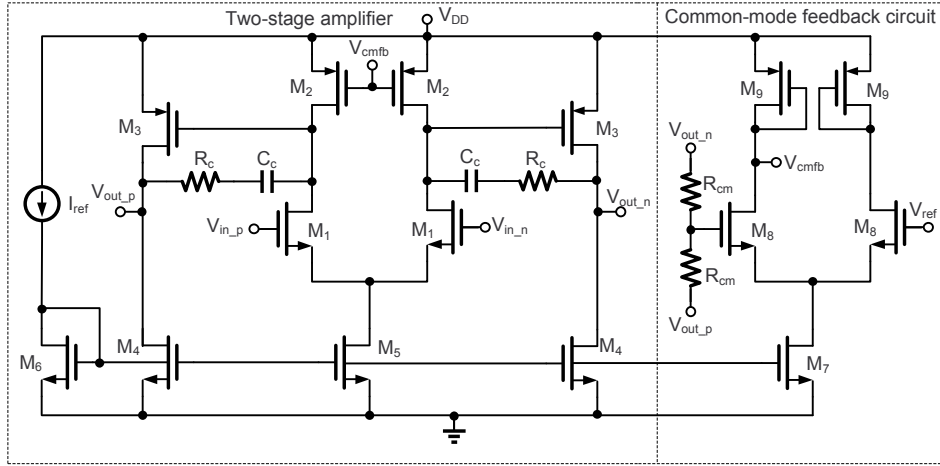


Figure 8.9: Fully differential two-stage amplifier implementation.

where $R_A = 280 \text{ k}\Omega$, and $C_A = 20 \text{ pF}$. Resistor R_B was implemented with a T-network structure to save die area.

8.3.2 Hysteretic Comparator

The comparator consumes only $50 \text{ }\mu\text{A}$ and has internal positive feedback [142] to generate a $\pm 10 \text{ mV}$ hysteresis window such that the CDA runs at approximately 380 kHz [143]. The schematic of the comparator is shown in Figure 8.10. The comparator consists of two stages: the input preamplifier to improve the comparator sensitivity and a positive feedback or decision stage. An output buffer (not shown) converts the output into a rail-to-rail signal. The transconductance g_m of M_1 determines the 1st stage gain, and the size W, L of M_1 determines the input capacitance C_{in} . To ensure high speed, the circuit has no high-impedance nodes other than the input and output nodes. The decision circuit uses positive feedback from the cross-gate connection of transistors M_4 to increase the gain of the decision element. The hysteresis window

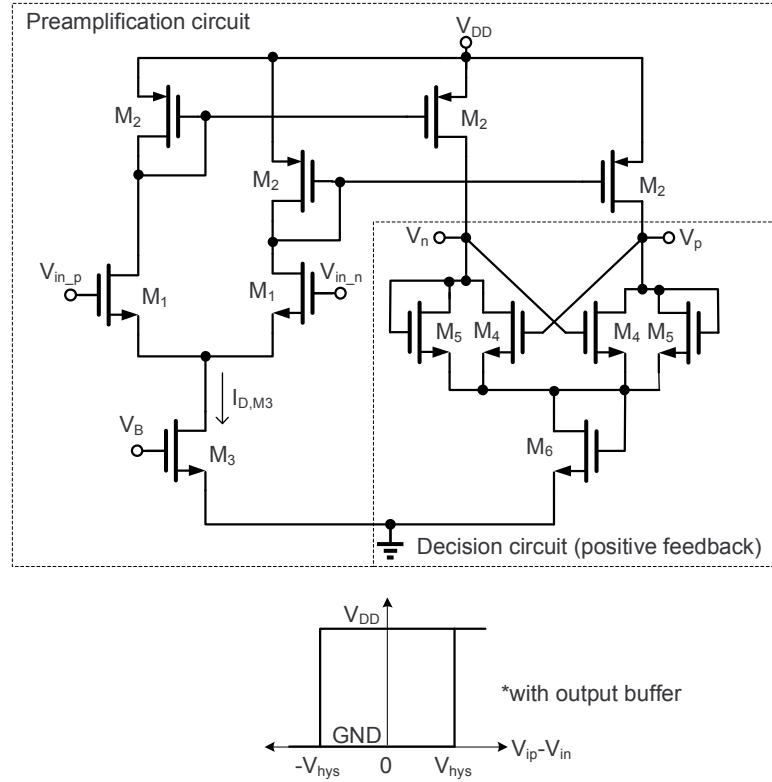


Figure 8.10: Hysteretic comparator implementation.

[142] is given by

$$V_{hys} = \frac{I_{D,M3} \frac{\beta_{M4}}{\beta_{M5}} - 1}{g_{m,M1} \frac{\beta_{M4}}{\beta_{M5}} + 1} \text{ for } \beta_{M4} \geq \beta_{M5}, \quad (8.7)$$

where

$$\beta_{M4,5} = K_n \frac{W_{M4,5}}{L_{M4,5}}. \quad (8.8)$$

Transistor M_6 increases the switching point to the desired DC common mode level. The output buffer is a NAND SR latch to convert the output of the decision circuit to a full swing signal.

Figure 8.11 shows the variation of the average switching frequency versus normalized input amplitude. As shown in the figure, the average switching frequency

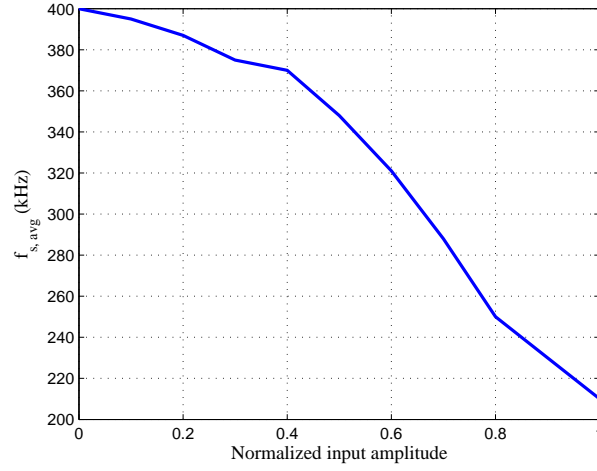


Figure 8.11: Average switching frequency versus normalized input amplitude ($\frac{V_{in,peak}}{V_{FS}}$, where $V_{FS} = 2.7$ V).

reduces from 400 kHz to 210 kHz as the peak input amplitude increases. This switching frequency variation could be reduced by monitoring the input amplitude and decreasing the comparator hysteresis as the input amplitude increases [137].

8.3.3 Output Power Stage

We designed the output buffer to minimize the dynamic power dissipation without degrading the propagation delay, and we reduced the short-circuit current with a non-overlap configuration [144]. In addition, we minimize conduction losses by reducing the CMOS on-resistance R_{on} . The calculations yielded a tapering factor between stages $T = 11$, a number of inverters $N = 4$ with and $R_{on} = 220$ m Ω . The dimensions of the PMOS power switch are $W = 27000$ μm and $L = 0.6$ μm and the dimensions of the NMOS power switch are $W = 9000$ μm and $L = 0.6$ μm .

8.3.4 Output Filter

The off-chip 2^{nd} -order LPF was designed with a cutoff frequency of 20 kHz, with $L = 45 \mu\text{H}$, $C = 1.5 \mu\text{F}$, and an 8Ω speaker. We chose a Butterworth filter approximation to achieve flat magnitude response within the audio band. The design of the integral sliding mode controller relies on the value of the elements in the low-pass filter as mentioned in Appendix C. Therefore, the proposed topology could be if necessary converted into a filterless architecture by calculating the coefficients of the integral sliding mode controller according to the speaker model [145] to obtain the highest performance possible.

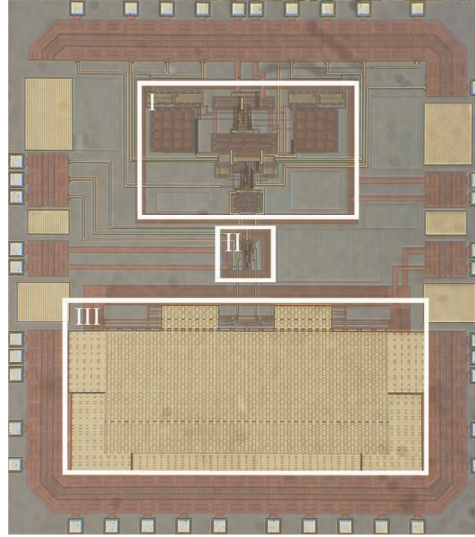


Figure 8.12: Class-D amplifier die micrograph, I controller (0.430mm^2), II comparator (0.033mm^2), and III output stage (1.190mm^2).

8.4 Experimental Results

The class D audio power amplifier was fabricated in $0.5 \mu\text{m}$ CMOS standard technology ($V_{THN} = 0.7 \text{ V}$, $V_{THP} = -0.9 \text{ V}$) and tested with a System One Dual

Domain Audio Precision instrument using a 2.7-V single voltage supply. The chip was encapsulated in a DIP 40 package. For details on measurement setup to obtain performance metrics of class-D audio amplifiers refer to section 7.3.5. Figure 8.12 shows the die micrograph of the fabricated CDA where blocks I, II, and III correspond to the ISMC, comparator, and output power stage, respectively. The total active area occupied by the class-D audio amplifier is approximately 1.65 mm^2 . The class-D

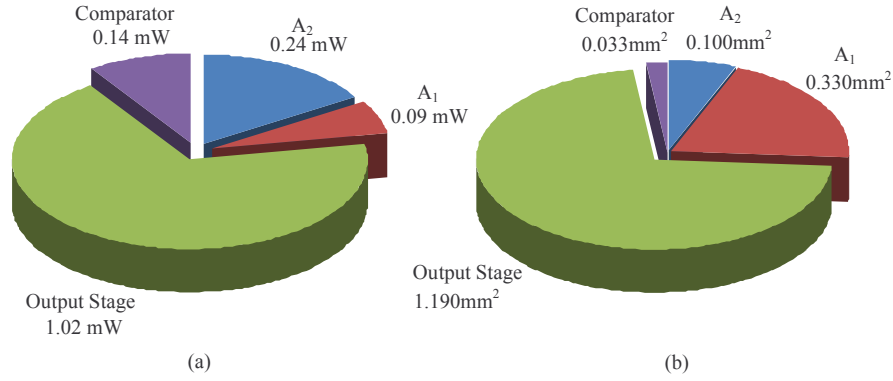


Figure 8.13: (a) Power and (b) area distribution of the proposed audio amplifier.

amplifier quiescent power distribution is shown in Figure 8.13(a). The output stage consumes 68% of the total quiescent power and the current-sense amplifier (A_2) consumes approximately half of the controller's power. The area distribution of the class-D audio amplifier is presented in Figure 8.13(b). The power stage occupies around two thirds of the total area. On the other hand, the comparator represents only 2% of the total area.

The output spectrum of the system with $V_{in} = 2.82 V_{pp}$ at 1 kHz is illustrated in Figure 8.14. As shown in the figure, the difference between the fundamental tone and the higher harmonic ($HD_3 = 3f_{in}$) is $> 70 \text{ dB}$.

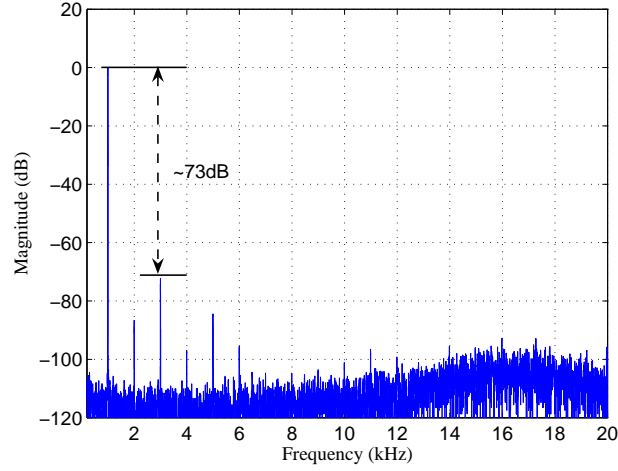
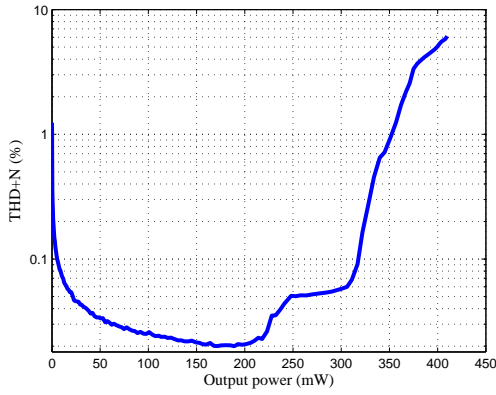
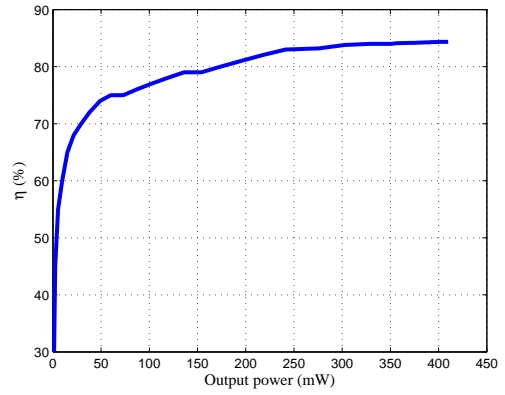


Figure 8.14: Class-D audio amplifier output FFT when $V_{in} = 2.82 V_{pp}$ at 1 kHz.



(a)



(b)

Figure 8.15: Class-D audio amplifier a) THD+N and b) efficiency versus output power.

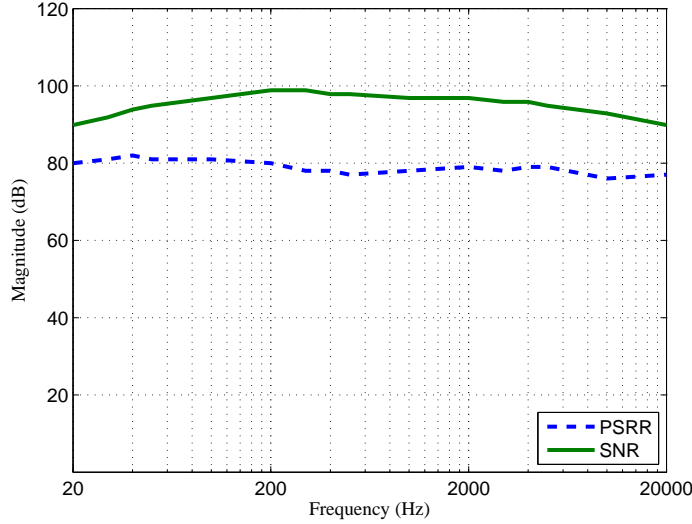


Figure 8.16: Class-D audio amplifier PSRR and SNR versus frequency.

The total harmonic distortion plus noise (THD+N) and the efficiency (η) performance of the CDA are shown in Figure 8.15. A THD+N of 0.02% and an efficiency of 84% were measured. The proposed system achieves a maximum output power of 410 mW for 7% THD+N. Thus, the system can provide approximately 90% of the maximum theoretical power. The voltage drop across R_s limits the maximum output voltage swing and hence limits the maximum power.

Figure 8.16 shows the PSRR and SNR versus frequency. A maximum PSRR of 82 dB was obtained while applying a sine-wave ripple of 100 mV_{pp} on the power supply. The SNR was measured with respect to 410 mW into an 8 Ω resistor [124] and was better than 90 dB across the entire audio band.

Class-D audio amplifiers may experience power-supply-induced intermodulation distortion (PS-IMD) [133]. We performed the power supply induced intermodulation test with an input voltage signal of 2 V_{pp} at 1 kHz and sinusoidal power-supply ripple of 300 mV_{pp} at 217 Hz superimposed on the DC level. A driver between the waveform

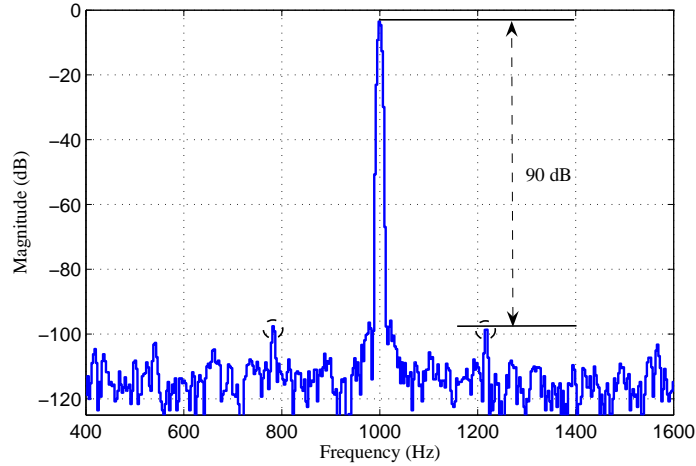


Figure 8.17: Power supply induced intermodulation distortion measurement.

generator and the VDD pin of the class-D amplifier provides the current required by the CDA as previously explained in section 7.3.9. Figure 8.17 shows that the difference between the intermodulation products (783 Hz and 1217 Hz) and the fundamental is approximately -90dBc.

Table 8.1 compares the performance of the presented CDA to that of the state-of-the-art audio amplifiers. We have included both controller's power P_c and quiescent power P_Q because we do not have complete information about the total quiescent power of previous works. Compared to previously published CDAs, the proposed clock-free current-controlled CDA consumes at least 30% less controller power.

8.5 Conclusion

This section has presented the design, implementation, and experimental results of a high PSRR clock-free current-controlled class-D amplifier. The proposed audio amplifier is based on integral sliding mode control to ensure robust operation and to provide zero steady-state error. The prototype has linearity and efficiency comparable to the state-of-the-art yet requires 30% less controller power and improves

the PSRR. Furthermore, we measured a power supply induced intermodulation distortion of approximately -90 dBc for an input voltage signal of 2 V_{pp} at 1 kHz and sinusoidal power-supply ripple of 300 mV_{pp} at 217 Hz superimposed on the DC level.

Table 8.1: Performance summary

Design	[132] ²⁰⁰⁵	[124] ²⁰⁰⁵	[122] ²⁰⁰⁸	[146] ²⁰⁰⁷	[137] ²⁰¹⁰	[64] ²⁰⁰⁷	[65] ²⁰⁰⁹	[147] ²⁰¹²	This Work ²⁰¹¹
P_c (mW)	-	50.00	-	-	40.00	5.40	0.68	-	0.47
P_Q (mW)	14.98	194.00	39.00	35.00	-	-	-	-	1.49
I_c (mA)	-	10.00	-	-	8.00	2.00	0.25	-	0.17
I_Q (mA)	4.70	12.00	7.80	7.00	-	-	-	3.02	0.55
PSRR (dB)	70	67	-	68	70	70	77	88	82
SNR (dB)	98	-	-	102	117	65	94	92	100
THD (%)	0.030	0.001	0.020	0.01	0.001	0.080	0.020	0.018	0.02
η (%)	76	88	87	85	85	91	89	85.5	84
Supply (V)	4.2	5.0	5.0	5.0	5.0	2.7	2.7	2.7-4.9	2.7
Load (Ω)	8	6	4	8	8	8	8	8	8
f_s (kHz)	410	450	3000	1800	600	500	450	320	380
P_{OUT} (mW)	700	10000	1000	1400	1400	200	250	1150	410
Area (mm ²)	0.44	10.15	6.00	-	6.00	4.70	1.49	1.01	1.65
Process	90nm DCMOS	0.6 μ m BCDMOS	0.35 μ m CMOS	-	0.7 μ m CMOS	0.5 μ m CMOS	0.5 μ m CMOS	180nm CMOS	0.5 μ m CMOS
Topology	PWM	$\Sigma\Delta$	$\Sigma\Delta$	$\Sigma\Delta$	Hysteretic	SMC	SMC	PWM	ISMC

9. SUMMARY

In this dissertation, design techniques to reduce circuit's area and/or quiescent power have been presented. A unified comparative study of capacitor-less LDO voltage regulators has been shown. Five CL-LDO regulator architectures were designed, fabricated, and tested under common design conditions. Trade-offs between the architectures and performance were highlighted.

Area reduction techniques for the output filter, output power stage, and compensator of the buck converter were proposed. The design and simulation results of a fully-integrated buck converter were presented. The use of additional post-fabrication processes has to be explored to boost the output inductor quality. Fully integrated power converters with high efficiency and good regulation will be necessary for future portable devices. Moreover, the design of an integrated single-input dual-output buck converter has been demonstrated. The converter presented high efficiency and good regulation performance. In addition, the design, implementation, and experimental results of a monolithic PWM voltage mode buck converter with compact Type-III compensation is shown. The prototype reduces the compensator's area by more than 60 %, and the total active chip area by approximately 25 % when compared with a similar design implemented with the conventional Type-III compensation scheme.

Finally, the design and implementation of a class-D audio amplifier using integral sliding mode control has been presented. The amplifier consumes 30 % less power than those of recently published works and has high PSRR performance within the audio band.

REFERENCES

- [1] J. Carbone, “Power management IC market will rebound,” *Digikey*, April 2013. [Online]. Available: <http://www.digikey.com>. [Accessed: May 9, 2013].
- [2] V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, New York: John Wiley and Sons Inc., 2006.
- [3] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd edition, Norwell: Kluwer Academic Publishers, 2001.
- [4] Z. Li and D. Pommerenke, “EMI specifics of synchronous DC-DC buck converters,” *IEEE International Symposium on Electromagnetics Compability*, pp. 711-714, August 2005.
- [5] *TPS60300 Single-Cell To 3.0-V/3.3-V, 20-mA Dual Output, High-Efficiency Charge Pump Datasheet*, Texas Instruments Inc., Dallas, Texas, March 2001.
- [6] *LM2665 Switched Capacitor Voltage Converter Datasheet*, Texas Instruments Inc., Dallas, Texas, May 2013.
- [7] G. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators*, New York: McGraw-Hill, Inc., 2009.
- [8] Y.-T. Lee, C.-L. Wei, and C.-H. Chen, “An integrated step-down DC-DC converter with Low output voltage ripple,” *IEEE Conference on Industrial Electronics and Applications*, pp. 1373-1378, July 2010.
- [9] G. A. Rincon-Mora, “Current efficient, low voltage, low drop-out regulators,” Ph.D dissertation, Georgia Institute of Technology, 1996. [Online]. Available: <http://users.ece.gatech.edu/rincon-mora/publicat/books/thesis/>. [Accessed: October 17, 2013].

- [10] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, E. Sánchez-Sinencio, “High PSR low drop-out regulator with feed-forward ripple cancellation technique,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 565-577, February 2009.
- [11] J. C. Teel, “Understanding power supply ripple rejection in linear regulators,” *Texas Instruments Inc.*, 2005. [Online]. Available: <http://www.ti.com>. [Accessed: October 17, 2013].
- [12] V. Gupta, G. Rincon-Mora, and P. Raha, “Analysis and design of monolithic, high PSR, linear regulators for SoC applications,” *IEEE International SOC Conference*, pp. 311-315, September 2004.
- [13] J. C. Teel, “Understanding noise in linear regulators,” *Texas Instruments Inc.*, 2005. [Online]. Available: <http://www.ti.com>. [Accessed: October 17, 2013].
- [14] S. Pithadia, “LDO noise demystified,” *Texas Instruments Inc.*, June 2009. [Online]. Available: <http://www.ti.com>. [Accessed: October 17, 2013].
- [15] W. Oh, B. Bakaloglu, C. Wang, and S.K. Hoon, “A CMOS low noise, chopper stabilized low-dropout regulator with current-mode feedback error amplifier,” *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 10, pp. 3006-3015, November 2008.
- [16] *TPS7A4700 36-V, 1-A, 4.17- μ V_{RMS}, RF LDO Voltage Regulator Datasheet*, Texas Instruments Inc., Dallas, Texas, July 2013.
- [17] B. S. Lee, “Understanding the terms and definitions of LDO voltage regulators,” *Texas Instruments Inc.*, October 1999. [Online]. Available: <http://www.ti.com>. [Accessed: October 17, 2013].
- [18] K. N. Leung and P. K. T. Mok, “A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation,” *IEEE Journal of Solid-*

- State Circuits*, vol. 38, no. 10, pp. 1691-1702, October 2003.
- [19] J. Panganiban, "Taking full advantage of very low dropout linear regulators," *Linear Technology Inc.*, December 2005. [Online]. Available: <http://www.linear.com>. [Accessed: October 17, 2013].
 - [20] A. Hastings, *The Art of Analog Layout*, Upper Saddle River, New Jersey: Prentice Hall, 2001.
 - [21] M. A. Rojas-Gonzalez, "Design and implementation of switching voltage integrated circuits based on sliding mode control," Ph.D Dissertation, Texas A&M Univeristy, 2009. [Online]. Available: <https://libcat.tamu.edu/>. [Accessed: July 8, 2013].
 - [22] J. Williams, "Minimizing switching regulator residue in linear regulator outputs," *Linear Technology Inc.*, July 2005. [Accessed: July 8, 2013].
 - [23] S. K. Lau, P. K. T. Mok, and K.N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE Journal of Solid-State Circuits*, vol.42, no.3, pp. 658-664, March 2007.
 - [24] H. C. Yang, M. S. Huang, and K. H. Chen, "High-PSR-bandwidth capacitor-free LDO regulator with $50\mu\text{A}$ minimized load current requirement for achieving high efficiency at light loads," *WSEAS Transactions on Circuits and Systems*, vol. 7, no. 5, pp. 428-437, May 2008.
 - [25] J. J. Chen, F. C. Yang, C. M. Kung, B. P. Lai, and Y. S. Hwang, "A capacitor-free fast-transient-response LDO with dual-loop controlled paths," *IEEE Asian Solid-State Circuit Conference*, pp. 364-367, November 2007.
 - [26] R. J. Milliken, J. Silva-Martínez, and E. Sánchez-Sinencio, "Full on chip CMOS low-dropout voltage regulator," *IEEE Transactions on Circuits and Systems I*,

- vol. 54, no. 9, pp. 1879-1890, September 2007.
- [27] P. S. Rao and K. S. R. Krishnaprasad, "A robust low-voltage on-chip LDO voltage regulator in 180 nm," *VLSI Design*, vol. 2008, Article ID 259281, 7 pages, 2008.
 - [28] L. G. Shen, Z.S. Yan, X. Zhang, and Y. F. Zhao, "A capacitor-less low-dropout regulator for SoC with bi-directional asymmetric buffer," *IEEE International Symposium on Circuits and Systems*, pp. 2677-2680, May 2008.
 - [29] T. Y. Man and P. K. T. Mok, "A high slew-rate push-pull output amplifier for low-quiescent current low-dropout regulators with transient-response improvement," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 9, pp. 755-759, September 2007.
 - [30] E. N. Y. Ho and P. K. T. Mok, "A capacitor-less CMOS active feedback low-dropout regulator with slew rate enhancement for portable on-chip application," *IEEE Transactions on Circuits and Systems II*, vol. 57, no. 2, pp. 80-84, February 2010.
 - [31] Z. Qianneng, W. Yongsheng, and L. Fengchang, "A capacitor-free CMOS LDO regulator with AC-boosting and active-feedback frequency compensation," *Journal of Semiconductors*, vol. 30, no. 4, pp. 1879-1890, April 2009.
 - [32] C. Zhan and W. H. Ki, "Output-capacitor-free adaptively biased low-dropout regulator for system-on-chips," *IEEE Transactions on Circuits and Systems I*, vol. 57, no. 5, pp. 1017-1028, May 2010.
 - [33] C. Zhen, and D. Ma, "Design of monolithic CMOS LDO Regulator with D^2 coupling and adaptive transmission control for adaptive wireless powered

- bio-implants,” *IEEE Transactions on Circuits and Systems I*, vol. 58, no. 10, pp. 2377-2387, October 2011.
- [34] V. Ivanov, “Design methodology and circuit techniques for any-load stable LDOs with instant load regulation and low noise,” *Advanced Analog Circuit Design*, New York: Springer, 2008.
- [35] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, “Area-efficient linear regulator with ultra-fast load regulation,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933-940, April 2005.
- [36] T. Y. Man, K. N. Leung, Ch. Y. Leung, P. K. T. Mok, and M. Chan, “Development of single-transistor-control LDO based on flipped voltage follower for SoC,” *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 5, pp. 1392-1401, June 2008.
- [37] P. Y. Or and K. N. Leung, “An output-capacitorless low-dropout regulator with direct voltage-spike detection,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 458-466, February 2010.
- [38] J. Guo and K. N. Leung, “A 6- μ W chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1896-1905, September 2010.
- [39] G. Blakiewicz, “Output-capacitorless low-dropout regulator using a cascoded flipped voltage follower,” *IET Circuits, Devices & Systems*, vol. 5, no. 5, pp. 418-423, September 2011.
- [40] V. Gupta and G. Rincon-Mora, “A 5mA 0.6 μ m CMOS miller-compensated LDO regulator with -27dB worst-case power-supply rejection using 60pF of on-

- chip capacitance,” *IEEE International Solid-State Circuits Conference*, pp. 520-521, February 2007.
- [41] C. Zhan and W. H. Ki, “A low dropout regulator for SoC with high power supply rejection and low quiescent current,” *IEEE 12th International Symposium on Integrated Circuits*, pp. 37-40, December 2009.
- [42] C. Zhan and W. H. Ki, “An output-capacitor-free cascode low-dropout regulator with low quiescent current and high power supply rejection,” *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 472-475, December 2010.
- [43] W. Xu, G. Wang, J. Jiang, X. Qi, and F. Zhang, “A high-PSR transient-enhanced output-capacitor less CMOS low-dropout regulator for SoC applications,” *International Journal of Electronics*, vol. 98, no. 10, pp. 1319-1332, October 2011.
- [44] E. N. Y. Ho and P. K. T. Mok, “Wide-loading-range fully integrated LDR with a power-supply ripple injection filter,” *IEEE Transactions on Circuits and Systems II*, vol. 59, no. 6, pp. 356-360, June 2012.
- [45] C. Cooper, “Fundamental of buck converter efficiency,” *Electronic Design*, May 2013. [Online]. Available: <http://electronicdesign.com>. [Accessed: August 1, 2013].
- [46] R. Nowakowski and N. Tang, “Efficiency of synchronous versus nonsynchronous buck converters,” *Texas Instruments Inc.*, 2009. [Online]. Available: <http://www.ti.com>. [Accessed: August 1, 2013].
- [47] Microsemi, “A simple current-sense technique eliminating a sense resistor,” *Microsemi*, July 1998. [Online]. Available: <http://www.microsemi.com>. [Accessed: July 30, 2013].

- [48] T. Y. Man, P. K. T. Mok, M. Chan, "An auto-selectable-frequency modulator for buck converters with improved light-load efficiency," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 440-626, February 2008.
- [49] E. Rogers, "Understanding buck power stages in switchmode power supplies," *Texas Instruments Inc.*, March 1999 [Online]. Available: <http://www.ti.com>. [Accessed: August 1, 2013].
- [50] M. D. Mulligan, B. Broach, and T. H. Lee, "A 3MHz low-voltage buck converter with improved light load efficiency," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 528-529, February 2007.
- [51] C. Zhang, "A dual-supply buck converter with improved light-load efficiency," Master's thesis, Texas A&M University, 2011. [Online]. Available: <https://libcat.tamu.edu/>. [Accessed: August 1, 2013].
- [52] D. Mattingly, "Design stable compensation networks for single phase voltage mode buck converters," *Intersil*, December 2013. [Online]. Available: <http://www.intersil.com>.
- [53] Exar, "Loop compensation of voltage-mode buck converters," *Exar Corp.*, October 2006. [Online]. Available: <http://www.exar.com>.
- [54] Exar, "Selecting Appropriate Compensation Type-II or Type-III," *Exar Corp.*, December 2006. [Online]. Available: <http://www.exar.com>.
- [55] S. Maniktala, "Voltage-mode, current-mode (and hysteretic control)," *Microsemi*, November 2012. [Online]. <http://www.microsemi.com>. [Accessed: September 16, 2013].
- [56] Texas Instruments, "Modeling, Analysis and Compensation of the Current-Mode Converter," *Texas Instruments Inc.*, September 1999. [Online].

<http://www.ti.com>. [Accessed: September 16, 2013].

- [57] H. P. Forghani-Zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC-DC converters," *IEEE 45th Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 577-580, August 2002.
- [58] J.-J. Chen, Y.-S. Hwang, J.-H. Su, and W.-C. Shih, "New current sensing circuit for hysteresis-current-controlled buck converters," *IEEE International Conference on Power Electronics and Drives Systems (PEDS)*, pp. 452-455, 2005.
- [59] P. K. T. Mok, "Tutorial T1: Embedded power-management circuits," presented at the *IEEE International Solid-State Circuits Conference*, San Francisco, CA, February 2007.
- [60] R. Miftakhudinov, "Synchronous buck regulator design using the TI TPS5211 high-frequency hysteretic controller," *Texas Instruments Inc.*, November 1999. [Online]. Available: <http://www.ti.com>. [Accessed: August 5, 2013].
- [61] C. H. Tso and J. C. Wu, "A ripple control buck regulator with fixed output frequency," *IEEE Power Electronics Letters*, vol. 1, no. 3, pp. 61-63, September 2003.
- [62] C. Song, "Optimizing accuracy of hysteretic control," *Power Electronics Technology*, February 2006. [Online]. Available: <http://powerelectronics.com>. [Accessed: August 5, 2013].
- [63] V. Utkin, J. Guldner, and J. Shi, *Sliding Mode Control in Electromechanical Systems*, Philadelphia: Taylor and Francis Inc., 1999.
- [64] M. A. Rojas-González and E. Sánchez-Sinencio, "Design of a class D audio amplifier IC using sliding mode control and negative feedback," *IEEE Transactions on Consumer Electronics*, vol. 53, no. 2, pp. 609-617, May 2007.

- [65] M. A. Rojas-González and E. Sánchez-Sinencio, "Two class-D audio amplifiers with 89/90 % efficiency and 0.02/0.03 % THD+N consuming less than 1mW of quiescent current power," *IEEE International Solid-State Circuits Conference*, February 2009, pp. 450-451.
- [66] M. A. Rojas-González and E. Sánchez-Sinencio, "Low-power high-efficiency class D audio power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3272-3284, December 2009.
- [67] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208-215, January 2007.
- [68] A. Parayandeh and A. Prodic, "Programmable analog-to-digital converter for low-power DC-DC SMPS," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 500-505, January 2008.
- [69] A. Syed, E. Ahmed, E. Alarcon, and D. Maksimovic, "Digital pulse width modulator architectures," *IEEE 35th Power Electronics Specialists Conference*, vol. 6, pp. 4689-4695, June 2004.
- [70] P. H. Lan, C. Y. Tseng, F. C. Yeh, and P. C. Huang, "A multi-mode digital controller with windowed ADC and self-calibrated DPWM for slew-enhanced switching converter," *IEEE Asian Solid Stage Circuit Conference (A-SSCC)*, pp. 1-4, November 2010.
- [71] T. Hegarty, "Benefits of multiphasing buck converters-Part 1," *EE Times*, November 2007. [Online]. Available: <http://www.eetimes.com>. [Accessed: August 7, 2013].

- [72] P. Xu, J. Wei, K. Yao, Y. Meng, and F. C. Lee, "Investigation of candidate topologies for 12 V VRM," *17th Annual IEEE Applied Power Electronics Conference (APEC)*, vol. 2, pp. 686-692, March 2002.
- [73] X. Zhou, P. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1172-1182, November 2000.
- [74] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal Solid-State Circuits*, vol. 39, no. 1, pp. 3-14, January 2004.
- [75] R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*, New York: John Wiley and Sons Inc., 1999.
- [76] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd Edition, New York: Oxford University Press, 2002.
- [77] H. P. Forghani-Zadeh and G. A. Rincon-Mora, "Low-power CMOS ramp generator circuit for DC-DC converters," *Journal of Low Power Electronics*, vol. 2, no. 3, pp. 437-441, December 2006.
- [78] D. Johns and K. Martin, *Analog Integrated Circuit Design*, New York: John Wiley and Sons Inc., 1997.
- [79] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Upper Saddle River, New Jersey: Prentice-Hall, 2001.
- [80] H. Dai and R. W. Knepper, "Modeling and experimental measurement of active substrate noise suppression in mixed signal 0.18- μ m BiCMOS technology," *IEEE*

- Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 6, pp. 826-836, June 2009.
- [81] M. Fortunato, "Temperature and voltage variation of ceramic capacitors, or hhy your 4.7 μ F capacitor becomes 0.33 μ F capacitor," *Maxim Integrated*, December 2012. [Online]. Available: <http://www.maximintegrated.com>. [Accessed: August 6, 2013].
- [82] J. Arrigo, "Input and output capacitor selection," *Texas Instruments Inc.*, February 2006. [Online]. Available: <http://www.ti.com>. [Accessed: August 6, 2013].
- [83] P. Hazucha, G. Schrom, J. Han, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karniket, V. De, and S. Borkar, "A 233 MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 838-845, April 2005.
- [84] S. Abedinpour, B. Bakkaloglu, and S. Kiaei, "A multistage interleaved synchronous buck converter with integrated output filter in 0.18 μ m SiGe process," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2164-2175, November 2007.
- [85] J. Y. Hung, W. Gao, and J. C. Hung, "Variable structure control: A survey," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 1, pp. 2-22, February 1993.
- [86] M. A. Rojas-Gonzalez, J. Torres, E. Sanchez-Sinencio, "Design of a fully-integrated buck voltage regulator using standard CMOS technology," *IEEE Third Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 1-4, March 2012.

- [87] G. Villar, E. Alarcon, F. Guinjoan, and A. Poveda, "Optimized design of MOS capacitors in standard CMOS technology and evaluation of their equivalent series resistance for power applications," *International Symposium on Circuits and Systems (ISCAS)*, pp. 451-454, May 2003.
- [88] P. Larsson, "Parasitic resistance in a MOS transistor used as on-chip decoupling capacitance," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 4, pp. 574-576, April 1997.
- [89] S. Musunuri and P. L. Chapman, "Design of low power monolithic DC-DC buck converter with integrated inductor," *IEEE 36th Power Electronics Specialists Conference*, pp. 1773-1779, June 2005.
- [90] J. Wibben and R. Harjani, "A high-efficiency DC-DC converter using 2 nH integrated inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 844-854, April 2008.
- [91] *EN5312Q 1 A Synchronous Buck Regulator with Integrated Inductor Datasheet*, Enpirion Inc., Hampton, New Jersey, June 2006.
- [92] C. Huang and P. K. T. Mok, "An 82.4% efficiency package-bondwire-based four-phase fully integrated buck converter with flying capacitor for area reduction," *IEEE International Solid-State Circuits Conference*, pp. 362-363, February 2013.
- [93] P. Kumar and M. Rojas-Gonzalez, "Novel 3-switch dual output buck voltage regulator," *21st Annual IEEE Applied Power Electronics Conference (APEC)*, pp. 467-473, March 2006.
- [94] P. Kumar, "Multiple output buck converter," U. S. Patent 7511463, April, 2009.

- [95] S. Chakraborty, A. K. Jain, and N. Mohan, "A novel converter topology for multiple individually regulated outputs," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 361-369, March 2006.
- [96] N. Chabini, I. Chabini, E. M. Aboulhamid, and Y. Savaria, "Methods for minimizing dynamic power consumption in synchronous designs with multiple supply voltages," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 3, pp. 346-351, March 2003.
- [97] J. Chang and M. Pedram, "Energy minimization using multiple supply voltages," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 4, pp. 436-443, December 1997.
- [98] K. Usami, M. Igarashi, F. Minami, T. Ishikawa, M. Kanzawa, M. Ichida, and K. Nogami, "Automated low-power technique exploiting multiple supply voltages applied to a media processor," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 463-472, March 1998.
- [99] A. P. Dancy, R. Amirtharajah, and A. Chandrakasan, "High-efficiency multiple-output DC-DC conversion for low-voltage systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 3, pp. 252-263, June 2000.
- [100] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, "A 200 mA 93% peak efficiency single-inductor dual-output DC-DC buck converter," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 526-527, February 2007.
- [101] M.A. Rojas-Gonzalez, J. Torres, E. Sanchez-Sinencio, and P. Kumar, "An integrated dual-output buck converter based on sliding mode control," *IEEE Third Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 1-4, March 2012.

- [102] M. Rojas-Gonzalez, J. Torres, P. Kumar, E. Sanchez-Sinencio, "Design of an integrated single-input dual-output 3-switch buck converter based on sliding mode control," *Analog Integrated Circuits and Signal Processing*, vol. 76, no. 3, pp. 307-319, September 2013.
- [103] A. M. Abo and P. R. Gray, "A 1.5 V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.
- [104] Texas Instruments, "1-MHz, 3.3V, High-Efficiency Synchronous Buck Converter With TPS43000 PMW Controller," *Texas Instruments, Inc.*, June 2002. [Online]. Available: <http://www.ti.com>.
- [105] *LM2854 4A 500 kHz / 1 MHz Synchronous SIMPLE SWITCHER Buck Regulator Datasheet*, Texas Instruments Inc., Dallas, Texas, April 2013.
- [106] M. Day, "Optimizing low-power DC-DC designs-external vs internal compensation," *Texas Instruments Inc.*, 2004. [Online]. Available: <http://www.ti.com>.
- [107] P. Y. Wu, S. Y. S. Tsui and P. K. T. Mok, "Area- and power-efficient monolithic buck converters with pseudo-type III compensation," *IEEE Journal of Solid-State Circuits*, vol.45, no.8, pp. 1446-1455, August 2010.
- [108] A. Veeravalli, J. Silva-Martinez, and E. Sanchez-Sinencio, "Transconductance amplifier structures with very small transconductances: a comparative design approach," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 6, pp. 770-775, September 2002.
- [109] P. Garde, "Transconductance cancellation for operational amplifier," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 310-311, June 1977.

- [110] J. Silva-Martinez and S. Solis-Bustos, "Design Considerations for high performance very-low-frequency filters," *IEEE International Symposium on Circuits and Systems*, pp. 648-651, July 1999.
- [111] C. Yoo, "A CMOS buffer without short-circuit power consumption," *IEEE Transactions on Circuits Systems II*, vol. 47, pp. 935-937, Sept. 2000.
- [112] H. Lee and P. K. T. Mok, "Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5 pp. 1136-1146, May 2005.
- [113] G. A. Cazzell, "Output impedance in PWM buck converter," Ph.D dissertation, Wright State University, 2009. [Online]. Available: <https://etd.ohiolink.edu>. [Accessed: October 17, 2013].
- [114] P. Y. Wu and P. K. T. Mok, "A Monolithic buck converter with near-optimum reference tracking response using adaptive-output-feedback," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2441-2450, November 2007.
- [115] P. J. Liu, W. S. Ye, J. N. Tai, H. S. Chen, J. H. Chen, and Y. J. Emery Chen, "A high-efficiency CMOS DC-DC converter with 9- μ s transient recovery time," *IEEE Transactions Circuits Systems I*, vol. 59, no. 3, pp. 575-583, March 2012.
- [116] D. Self, *Audio Power Amplifier Design Handbook*, 4th Edition, Oxford, UK: Newnes-Elsevier, 2006.
- [117] M. Berkhout, L. Breems, and E. van Tuijil, "Audio at low and high power," *IEEE European Solid-State Conference (ESSCIRC)*, pp. 40-49, September 2008.

- [118] B. Forejt, "Tutorial T1: Fundamentals of class-D amplifier operation & design," *presented at the IEEE International Solid-State Circuits Conference*, San Francisco, CA, February 2008.
- [119] E. Gaalaas, "Class D audio amplifiers: what, why, and how," *Analog Devices*, June 2006. [Online]. Available: <http://www.analog.com>. [Accessed: August 16, 2013].
- [120] J. Honda and J. Adams, "Class D audio amplifier basics," *International Rectifier*, February 2005. [Online]. Available: <http://www.irf.com>. [Accessed: August 16, 2013].
- [121] Y. B. Quek, "Class-D LC filter design," *Texas Instruments Inc.*, January 2008. [Online]. Available: <http://www.ti.com>. [Accessed: August 17, 2013].
- [122] C. Lin, Y. Lee, and W. Chen, "A 1.5 bit 5th order CT/DT delta sigma class D amplifier with power efficiency improvement," *IEEE International Symposium on Circuits and Systems*, pp. 280-283, May 2008.
- [123] Y. Fujimoto, P. L. Re, and M. Miyamoto, "A delta-sigma modulator for a 1-bit digital switching amplifier", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp.1865-1871, September 2005.
- [124] E. Gaalaas, B. Y. Liu, and N. Nishimura, "Integrated stereo delta-sigma class D audio amplifier," *IEEE International Solid-State Circuits Conference*, pp. 120-121, February 2005.
- [125] V. I. Utkin, "Sliding mode control design principles and applications to electric drives," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 1, pp. 23-36, February 1993.

- [126] J. F. Silva, "PWM audio power amplifiers: Sigma delta versus sliding mode control," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 359-362, September 1998.
- [127] R. Cellier, G. Pillonet, A. Nagari, and N. Abouchi, "An review of fully digital audio class D amplifiers topologies," *IEEE Circuits and Systems and Taisa Conference*, pp. 1-4, June 2009.
- [128] V. Adrian, J. S. Chang, and B. H. Gwee, "A low-voltage micropower digital class-D amplifier modulator for hearing aids," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 2, pp. 337-349, February 2009.
- [129] M. Score and D. Dapkus, "Filterless class D simplifies audio amplifier design," *EE Times*, October 2000. [Online]. Available: <http://www.eetimes.com>. [Accessed: August 20, 2013].
- [130] R. Palmer, "Guidelines for measuring audio power amplifier performance," *Texas Instruments Inc.*, October 2001. [Online]. Available: <http://www.ti.com>. [Accessed: October 5, 2013].
- [131] B. Hofer, "Measuring switch-mode power amplifiers," *Audio Precision Inc.*, October 2003. [Online]. Available: <http://ap.com>. [Accessed: October 5, 2013].
- [132] B. Forejt, V. Rentala, J. D. Arteaga, and G. Burra, "A 700+-mV class D design with direct battery hookup in a 90-nm process," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1880-1887, September 2005.
- [133] T. Ge and J. S. Chang, "Modeling and technique to improve PSRR and PS-IMD in analog PWM Class-D amplifiers," *IEEE Transactions on Circuits and Systems II*, vol. 55, no. 6, pp. 512-516, June 2008.

- [134] J. Torres, A. Colli-Menchi, M. A. Rojas-González, and E. Sánchez-Sinencio, "A low-power high-PSRR clock-free current-controlled class-D audio amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1553-1561, July 2011.
- [135] M. T. Tan, J. S. Chang, H. C. Chua, and B. H. Gwee, "An investigation on the parameters affecting total harmonic distortion in a CDA," *IEEE Transactions on Circuits and Systems I*, vol. 50, no. 10, pp. 1304-1315, October 2003.
- [136] W. Shu and J. S. Chang, "THD of closed-loop analog PWM class-D amplifier," *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 6, pp. 1769-1777, July 2008.
- [137] J. Lu and R. Gharpurey, "A self oscillating class D audio amplifier with 0.0012% THD+N and 116.5 dB dynamic range," *IEEE Custom Integrated Circuits Conference*, pp. 1-4, September 2010.
- [138] S. K. Mazumder and S. L. Kamisetty, "Design and experimental validation of a multiphase VRM Controller," *IEE Proceedings on Electric Power Applications*, vol. 152, no. 5, pp. 1076-1084, September 2005.
- [139] M. Lopez, L. G. De Vicuna, M. Castilla, P. Gaya, and O. Lopez, "Current distribution control design for paralleled DC/DC converters using sliding-mode control," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 2, pp. 419-428, April 2004.
- [140] M. Castilla, L. G. De Vicuna, J. M. Guerrero, J. Matas, and J. Miret, "Design of voltage-mode hysteretic controllers for synchronous buck converters supplying microprocessor loads," *IEE Proceedings on Electric Power Applications*, vol. 152, no. 5, pp. 1171-1178, September 2005.

- [141] S. K. Mazumder, A. H. Nayfeh, and D. Borojevic, "Robust control of parallel DC-DC buck converters by combining integral-variable-structure and multiple-sliding-surface control schemes," *IEEE Transactions on Power Electronics*, vol. 17, no. 3, pp. 428-437, May 2002.
- [142] R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, 2nd Edition, Wiley-IEEE Press, 2008.
- [143] S. Tan, Y. M. Lai, M. K. H. Cheung, and C. K. Tse, "On the practical design of a sliding mode voltage controlled buck converter," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 425-437, March 2005.
- [144] J. Chang, M. Tan, Z. Cheng, and Y. Tong, "Analysis and design of power efficient class D amplifier output stages," *IEEE Transactions on Circuits and Systems I*, vol. 47, no. 6, pp. 897-902, June 2000.
- [145] T. Ge and J. S. Chang, "Filterless class D amplifiers: power-efficiency and power dissipation," *IET Circuits, Devices & Systems*, vol. 4, no. 1, pp. 48-56, January 2010.
- [146] *SSM2304 2W Filterless Class-D Stereo Audio Amplifier Datasheet*, Analog Devices Inc., Norwood, Massachusetts, April 2007.
- [147] Y. Choi, W. Tak, Y. Yoon, J. Roh, S. Kwon, J. Koh, "A 0.0018% THD+N, 88-dB PSRR PWM class-D amplifier for direct battery hookup," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 454-463, February 2012.
- [148] V. Utkin, "Variable structure systems with sliding mode," *IEEE Transactions on Automatic Control*, vol. 22, no. 2, pp. 212-222, April 1977.
- [149] H. K. Khalil, *Nonlinear Systems*, 3rd Edition, Upper Saddle River, New Jersey: Prentice Hall, 2002.

- [150] K. Ogata, *Modern Control Engineering*, 3rd Edition, Upper Saddle River, New Jersey: Prentice Hall, 1998.
- [151] R. C. Dorf and R. H. Bishop, *Modern Control Systems*, 10th Edition, Upper Saddle River, New Jersey: Prentice Hall, 2005.
- [152] C. Chen, *Linear System Theory and Design*, 3rd Edition, New York: Oxford University Press, 1999.
- [153] F. B. Cunha, D. J. Pagano, and U. F. Moreno, "Sliding bifurcations of equilibria in planar variable structure systems," *IEEE Transactions on Circuits and Systems I*, vol. 50, no. 8, pp. 1129-1134, August 2003.

APPENDIX A

LDO VOLTAGE REGULATOR PERFORMANCE DEFINITIONS

This appendix provides low drop-out voltage regulator performance definitions.

- **Stability:** it is quantified by measuring the phase margin at the loop's unity gain frequency.
- **Load transient:** quantifies the peak output-voltage excursion and signal settling time when the load-current is stepped.
- **Load regulation:** quantifies the voltage variation at the output when a change in the load-current happens but it is measured once the output voltage is in steady-state.
- **Power supply rejection:** refers to the amount of voltage ripple at the output of the LDO coming from the ripple at the input.
- **Line transient:** measures the output voltage variation in response to a voltage step at the input of the LDO regulator.
- **Line regulation:** quantifies the voltage variation at the output when a change in the input voltage happens but it is measured once the output voltage is in steady-state.
- **Noise:** refers to the thermal and flicker noise in transistors and resistors in LDO voltage regulator .
- **Drop-out voltage:** it is the minimum difference between the input and output voltages at which the circuit ceases to regulate.

- **Quiescent current:** it is the difference between the input current of the LDO voltage regulator and load current.
- **Efficiency:** it is defined as the ratio of the output power over the input power.

APPENDIX B

FUNDAMENTALS OF SLIDING MODE CONTROL*

This appendix presents the fundamentals of sliding mode control (SMC) theory. It begins with an introductory example to illustrate its principles of operation, and to highlight its main characteristics. Additionally, a formal description of the sliding mode controller, and the switching function, is given. Furthermore, the analysis of stability, based on the Lyapunov function approach and the equivalent control approach, is explained. Finally, the derivation of the switching function and the stability proof, for the particular case of the second-order low-pass filter employed in the design of the systems described in this dissertation, are detailed.

B.1 An Introductory Example

The first developments of sliding mode control (SMC) occurred in the 1950s as a consequence of the analysis of discontinuous variable structure systems (VSS). A variable structure system consists of a set of continuous subsystems together with a switching logic. Therefore, the variable structure control (VSC) with sliding modes consists on selecting the parameters of each one of these substructures to define the switching logic of the system. The most outstanding feature of variable structure control is its ability to result in very robust control systems, insensitive to parametric uncertainty, and external disturbances [63], [85], [148], [149].

The basic idea of variable structure control with sliding modes, or simply sliding mode control, can be illustrated by analyzing the second order system shown in

*Reprinted with permission from “Design and implementation of switching voltage integrated circuits based on sliding mode control,” by M. A. Rojas-González, Ph.D Dissertation, Texas A&M University, August 2009.

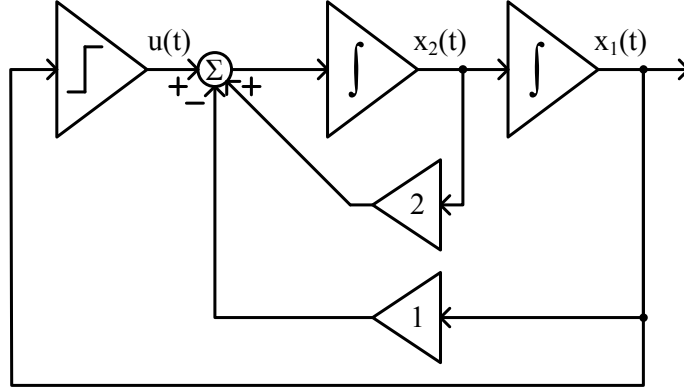


Figure B.1: Model of a simple variable structure system.

Figure B.1. The system can be expressed in terms of its state variables as

$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ -1 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} u(t) \quad (\text{B.1})$$

where

$$u(t) = \begin{cases} 4 & \text{when } s(x_1, x_2, t) > 0 \\ -4 & \text{when } s(x_1, x_2, t) < 0 \end{cases} \quad (\text{B.2})$$

and $s(x_1, x_2, t)$, defined as

$$s(x_1, x_2, t) = x_1(t) \left(\frac{1}{2}x_1(t) + x_2(t) \right) \quad (\text{B.3})$$

represents the switching function, which will be defined later in the appendix.

Therefore, the second-order system, in equation (B.1), is analytically defined in two regions of the phase plane, i.e. the x_1 - x_2 plane, by two different mathematical

models. The first model, when $s(x_1, x_2, t) < 0$, is

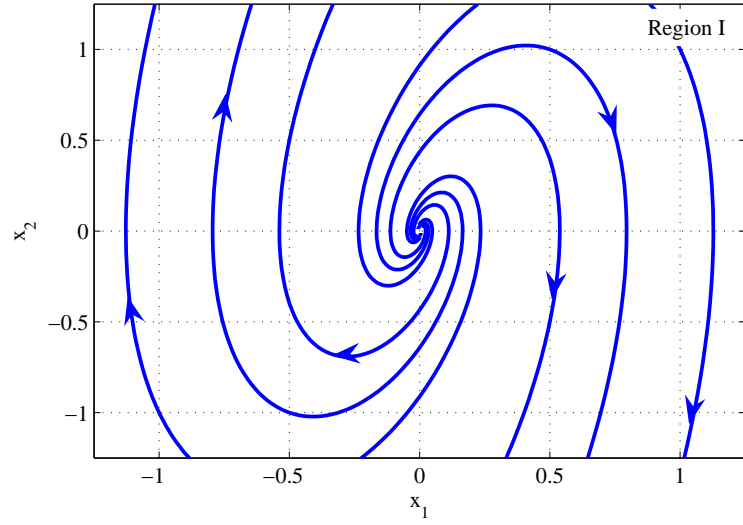
$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ -5 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} \quad (\text{B.4})$$

and the second model, when $s(x_1, x_2, t) > 0$, is

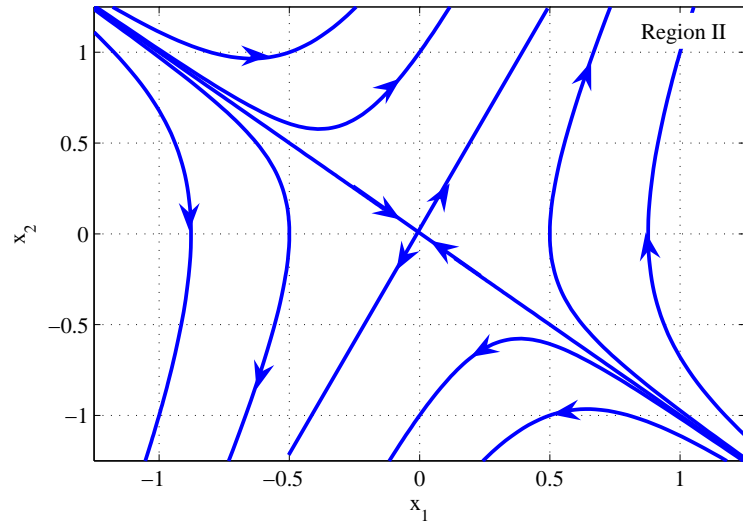
$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ 3 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} \quad (\text{B.5})$$

The phase portraits, i.e. the trajectories of the state-space variables in the phase plane for different initial conditions, for the models in equations (B.4) and (B.5) are shown in Figure B.2. Figure B.2(a) corresponds to the state-space model in equation (B.4) and represents the first region of operation, i.e. region I. Observe that the equilibrium point is an unstable focus [149], i.e. positive eigenvalues with imaginary part, at the origin. On the other hand, the second region of operation, or region II, is represented by the phase portrait, of the state space model expressed in equation (B.5), in Figure B.2(b). Notice that, in this case, its equilibrium point, at the origin, is a saddle point [149], i.e. one positive and one negative real eigenvalues, and therefore, it is stable for only one trajectory.

The variable $s(x_1, x_2, t)$ in equation (B.3) describes lines dividing the phase plane into the regions of operation where $s(x_1, x_2, t)$ has different sign. Such lines are called switching lines and $s(x_1, x_2, t)$ is called the switching function. The switching lines occur whenever $s(x_1, x_2, t) = 0$ and are known as the switching surfaces. Hence, the feedback control $u(t)$ switches according to the sign of $s(x_1, x_2, t)$. For example, the switching function in equation (B.3) defines the phase portrait, of the second-order system in equation (B.1), as illustrated in Figure B.3. The phase plane is divided into



(a)



(b)

Figure B.2: Phase portraits of the second-order system in equation (B.1) for (a) Region I when $s(x_1, x_2, t) < 0$ and (b) Region II when $s(x_1, x_2, t) > 0$.

regions of operation, each one of them linked to the state-space systems in equations (B.4) and (B.5). The switching function controls the switching logic to stabilize the system for any given initial condition.

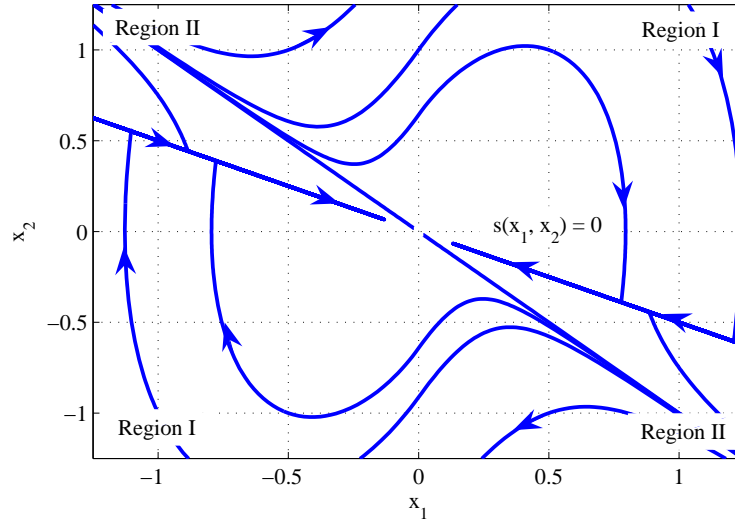


Figure B.3: Phase portrait of the second-order system in equation (B.1) with sliding mode.

The phase trajectories, plotted in the phase portrait of Figure B.3, correspond to the two modes of operation of the system. The first part is the reaching mode, also called nonsliding mode, in which a trajectory starting at any initial condition moves toward a switching line and reaches the line in finite time. The second part is the sliding mode, in which the trajectory asymptotically tends to the origin of the phase plane. This displacement is called sliding because in the ideal case, the system switches at infinite frequency, causing a sliding behavior of the particular trajectory. During the control process, the variable structure system, in equation (B.1), varies from one structure to another, thus earning the name variable structure control. The control is also called sliding mode control to emphasize the important role of sliding

mode [63], [85], [148], [149].

B.2 Sliding Mode Controller

The switching function represents the sliding mode controller, i.e. the control law, of a variable structure system. Hence, if the variable structure system is expressed in the controllable canonical form [150]-[152] as

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}u(t) \quad (\text{B.6})$$

$$y(t) = \mathbf{C}\mathbf{x}(t) \quad (\text{B.7})$$

where

$$\mathbf{x}(t) = \begin{pmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_{n-1}(t) \\ x_n(t) \end{pmatrix} \quad (\text{B.8})$$

$$\mathbf{A} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -a_1 & -a_2 & -a_3 & \cdots & -a_n \end{pmatrix} \quad (\text{B.9})$$

$$\mathbf{B} = \begin{pmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{pmatrix} \quad (\text{B.10})$$

$$\mathbf{C} = \begin{pmatrix} c_1 & c_2 & \cdots & c_n \end{pmatrix} \quad (\text{B.11})$$

and $x_n(t)$, $u(t)$, and $y(t)$ are the state variables of the system, the control input, and the output of the system, respectively. Then, the function

$$\mathbf{s}(\mathbf{x}, t) = k_1 x_1(t) + k_2 x_2(t) + \cdots + k_n x_n(t) \quad (\text{B.12})$$

defines the switching surfaces in the n^{th} space, when $\mathbf{s}(\mathbf{x}, t) = 0$. The coefficients in the switching function define the characteristic equation of the sliding mode if the system model is described in the controllable canonical form [63], [85], [148], [149].

In the same way, the control law can be designed such that the output of the system $y(t)$ asymptotically tracks a reference signal $r(t)$. Therefore, if the variable structure system is rewritten with

$$\begin{pmatrix} \dot{e}_1(t) \\ \dot{e}_2(t) \\ \vdots \\ \dot{e}_{n-1}(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \end{pmatrix} \begin{pmatrix} e_1(t) \\ e_2(t) \\ \vdots \\ e_n(t) \end{pmatrix} \quad (\text{B.13})$$

where $e_1(t) = r(t) - y(t)$ is the error function, $e_n(t)$ is the control input, and n is the order of the system to be controlled. The control input, defined in equation (B.14), is the linear combination of all canonical state variables [85], [149], and whose

coefficients are chosen in such way that the polynomial, in equation (B.15), meets the Hurwitz criterion [150]-[152], i.e. all its roots have negative real part.

$$e_n(t) = -[k_1 e_1(t) + k_2 e_2(t) + \dots + k_{n-1} e_{n-1}(t)] \quad (\text{B.14})$$

$$P(s) = k_n s^{n-1} + k_{n-1} s^{n-2} + \dots + k_1 \quad (\text{B.15})$$

Then, the switching function in equation (B.16) represents the $(n-1)$ dimensional surface where the points of discontinuity merge [85].

$$\mathbf{s}(\mathbf{e}, t) = k_1 e_1(t) + k_2 e_2(t) + \dots + k_{n-1} e_{n-1}(t) + k_n e_n(t) = 0 \quad (\text{B.16})$$

B.3 Stability Analysis

Variable structure systems operating under sliding mode control consist of two parts, the reaching mode and the sliding mode. Therefore, the analysis of stability must demonstrate that (1) the trajectory of a given state moves toward and reaches the sliding surface, and (2) the state asymptotically tends to the equilibrium point of the system.

B.3.1. Reaching Mode Condition

The reaching mode condition can be analyzed by employing the Lyapunov function approach [85]. Hence, by choosing the Lyapunov function candidate

$$\mathbf{v}(\mathbf{x}, t) = \frac{1}{2} \mathbf{s}^T(\mathbf{x}, t) \mathbf{s}(\mathbf{x}, t) \quad (\text{B.17})$$

a global reaching condition is given by

$$\frac{d}{dt} \mathbf{v}(\mathbf{x}, t) < 0 \quad (\text{B.18})$$

when $\mathbf{s}(\mathbf{x}, t) \neq 0$ [85], [149].

B.3.2. Sliding Mode Condition

The convergence of a variable structure system to its equilibrium point, also called sliding equilibrium point or quasiequilibrium point [153], can be found by analyzing the qualitative behavior [149], i.e. calculating the eigenvalues, of the equivalent variable structure system when

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}u_{eq}(t) = 0 \quad (\text{B.19})$$

$$\mathbf{s}(\mathbf{x}, t) = 0 \quad (\text{B.20})$$

where $u_{eq}(t)$ is the equivalent control input that describes the dynamics of the sliding mode as the average value of the discontinuous input $u(t)$ [153]. Hence, if the switching function $\mathbf{s}(\mathbf{x}, t)$ is expressed in terms of the state variables as

$$\mathbf{s}(\mathbf{x}, t) = \mathbf{D}(\mathbf{x}, t) + \mathbf{E}(\mathbf{x}, t)u(t) \quad (\text{B.21})$$

then, the equivalent control can be found when the state trajectory stays on the switching surface $\mathbf{s}(\mathbf{x}, t) = 0$ [85]. Therefore, differentiating $\mathbf{s}(\mathbf{x}, t)$ with respect to time gives

$$\frac{d}{dt}\mathbf{s}(\mathbf{x}, t) = \frac{\partial}{\partial \mathbf{x}} \frac{d}{dt}\mathbf{D}(\mathbf{x}, t) + \frac{\partial}{\partial \mathbf{x}} \frac{d}{dt}\mathbf{E}(\mathbf{x}, t)u(t) \quad (\text{B.22})$$

and solving equation (B.22) for $u(t)$ yields the equivalent control input $u_{eq}(\mathbf{x}, t)$ [85] as

$$\mathbf{u}_{eq}(\mathbf{x}, t) = - \left(\frac{\partial}{\partial \mathbf{x}} \frac{d}{dt}\mathbf{E}(\mathbf{x}, t) \right)^{-1} \frac{\partial}{\partial \mathbf{x}} \frac{d}{dt}\mathbf{D}(\mathbf{x}, t) \quad (\text{B.23})$$

B.4 Practical Derivation of the Switching Function and Stability Analysis

If the variable structure system, as described in previous chapters, is defined by the second-order state-space system given by

$$\begin{pmatrix} \frac{d}{dt} i_L(t) \\ \frac{d}{dt} v_C(t) \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} u(t) \quad (\text{B.24})$$

with an error function $e_1(t) = v_{REF}(t) - v_C(t)$, then, from equations (B.13) and (B.14), we have

$$\frac{d}{dt} e_1(t) = e_2(t) \quad (\text{B.25})$$

$$e_2(t) = -k_1 e_1(t) \quad (\text{B.26})$$

and the switching function $s(e_1, e_2, t)$, from equation (B.16), is defined as

$$s(e_1, e_2, t) = k_1 e_1(t) + k_2 e_2(t) \quad (\text{B.27})$$

where k_1 and k_2 must be chosen such that the polynomial $P(s) = k_2 s + k_1$, from equation (B.15), is Hurwitz. Therefore, the control input $u(t)$ switches according to

$$u(t) = \begin{cases} v_{DD} & \text{when } s(e_1, e_2, t) > 0 \\ v_{SS} & \text{when } s(e_1, e_2, t) < 0 \end{cases} \quad (\text{B.28})$$

Hence, the switching function in equation (B.27) can be rewritten as a function of the state-space variables as

$$s(e_1, e_2, t) = e_1(t) + \alpha e_2(t) = v_{REF}(t) - v_C(t) - \alpha \frac{d}{dt} v_C(t) \quad (\text{B.29})$$

and the derivative of the switching function, from equation (B.22), is

$$\begin{aligned}\dot{s}(e_1, e_2, t) &= \frac{1}{C} \left(\frac{\alpha}{RC} - 1 \right) i_L(t) \\ &- \left[\frac{1}{RC} \left(\frac{\alpha}{RC} - 1 \right) - \frac{\alpha}{LC} \right] v_C(t) - \frac{\alpha}{LC} u(t)\end{aligned}\quad (\text{B.30})$$

The analysis of stability based on the Lyapunov function approach assumes the control signal $u(t)$ can be decomposed into two parts

$$u(t) = u_{eq}(t) + u_{nl}(t) \quad (\text{B.31})$$

where $u_{eq}(t)$ is the equivalent control input, and $u_{nl}(t)$ is the nonlinear switching function, i.e., the high-frequency component. Therefore, the equivalent control input, defined in equation (B.23), for this particular case is

$$u_{eq}(t) = \left(\begin{array}{cc} \frac{L}{\alpha} \left[\frac{\alpha}{RC} - 1 \right] & 1 - \frac{L}{\alpha R} \left[\frac{\alpha}{RC} - 1 \right] \end{array} \right) \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} \quad (\text{B.32})$$

hence, substituting equations (B.28) and (B.32) into equation (B.30) yields

$$\dot{s}(e_1, e_2, t) = - \frac{\alpha}{CL} u_{nl}(t) \quad (\text{B.33})$$

Therefore, the Lyapunov function candidate, from equation (B.17), becomes

$$v(e_1, e_2, t) = \frac{1}{2} s^2(e_1, e_2, t) \quad (\text{B.34})$$

and the global reaching condition is

$$\frac{d}{dt}v(e_1, e_2, t) = s(e_1, e_2, t)\dot{s}(e_1, e_2, t) = s(e_1, e_2, t) \left(-\frac{\alpha}{CL}u_{nl}(t) \right) < 0 \quad (\text{B.35})$$

when $s(e_1, e_2, t) \neq 0$. Simplifying and rearranging we get

$$s(e_1, e_2, t)u_{nl}(t) > 0 \quad (\text{B.36})$$

Hence, based on equations (B.28) and (B.31), when $s(e_1, e_2, t) > 0$, then $u(t) = v_{DD}$ and thus $v_{DD} = u_{eq} + u_{nl}$, therefore, if $v_{DD} - u_{eq} > 0$, it implies that $u_{nl} > 0$ and

$$[s(e_1, e_2, t)][u_{nl}(t)] > 0 \quad (\text{B.37})$$

for $s(e_1, e_2, t) > 0$. On the other hand, when $s(e_1, e_2, t) < 0$, then $u(t) = v_{SS}$, so $v_{SS} = u_{eq} + u_{nl}$, this implies that if $v_{SS} - u_{eq} < 0$, therefore $u_{nl} < 0$ and

$$[-s(e_1, e_2, t)][-u_{nl}(t)] > 0 \quad (\text{B.38})$$

for $s(e_1, e_2, t) < 0$. Then, if $v_{SS} < u_{eq} < v_{DD}$ holds, the control law ensures the reaching condition. Since we know that u_{eq} is the low-frequency average signal that tracks the reference input v_{ref} , then the last inequality is true.

On the other hand, the sliding mode condition can be proven if the sliding equilibrium point of the equivalent control system is found, and its eigenvalues have negative real part. Therefore, the equivalent input control input in equation (B.32)

is substituted in the state-space model in equation (B.24) as

$$\begin{pmatrix} \frac{d}{dt}i_L(t) \\ \frac{d}{dt}v_C(t) \end{pmatrix} = \begin{pmatrix} \frac{1}{\alpha} \left(\frac{\alpha}{RC} - 1 \right) & -\frac{1}{\alpha R} \left(\frac{\alpha}{RC} - 1 \right) \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} \quad (\text{B.39})$$

Then, as shown in equations (B.19) and (B.20), if the resulting equivalent control system, along with the switching function are solved, when they are equal to zero, the sliding equilibrium point yields

$$[v_C(t), i_L(t)] = \left[v_{REF}(t), \frac{v_{REF}(t)}{R} \right] \quad (\text{B.40})$$

The sliding equilibrium point corresponds to the desired voltage $v_{REF}(t)$ at the output second-order low-pass filter. Assuming that $v_C(t) = v_{OUT}(t)$, the sliding mode controller will track the trajectory of the input signal $v_{REF}(t)$. Similarly, the value of the inductor current $i_L(t)$ will be defined by the output voltage divided by the resistive load.

The value of the eigenvalues in the equivalent control model can be calculated to show that the system converges to the sliding equilibrium point. Therefore, solving for $v_C(t)$ in equation (B.29), when $s(e_1, e_2, t) = 0$, and substituting into the equivalent control model expressed in equation (B.39), the eigenvalues (λ) of the equivalent system are

$$\lambda_{1,2} = \left(-\frac{1}{\alpha}, -\frac{1}{RC} \right) \quad (\text{B.41})$$

Thus, the system is asymptotically stable since its sliding equilibrium point is a node whose eigenvalues are real and negative, for $\alpha > 0$.

Furthermore, the final value theorem (FVT) [151] can be used in order to calculate the steady-state of the model to verify that system under sliding mode is in fact a

tracking system. In general, the final value of a given system $y(t)$ can be determined as

$$\lim_{t \rightarrow \infty} y(t) = \lim_{s \rightarrow 0} sY(s) \quad (\text{B.42})$$

The transfer function of the equivalent control model, resulting from the combination of equations (B.29) and (B.39), is

$$\frac{V_{OUT}(s)}{V_{REF}(s)} = \frac{1}{(\alpha s + 1)(RCs + 1)} \quad (\text{B.43})$$

which agrees with the results given in equation (B.41) for the eigenvalues of the equivalent control model.

Applying the final value theorem to equation (B.43) with a step input of value v_{STEP} to the system we have

$$\begin{aligned} \lim_{t \rightarrow \infty} v_{OUT}(t) &= \lim_{s \rightarrow 0} sV_{OUT}(s) \\ &= \lim_{s \rightarrow 0} \left(\frac{s}{(\alpha s + 1)(RCs + 1)} \right) \left(\frac{V_{STEP}}{s} \right) \\ &= v_{STEP} \end{aligned} \quad (\text{B.44})$$

Hence, the equivalent control model tracks the input input step signal v_{STEP} .

APPENDIX C

STABILITY ANALYSIS OF THE CLASS-D AUDIO AMPLIFIER*

This appendix derives the equivalent control model and the stability analysis of the proposed class-D audio amplifier operating under integral sliding-mode control. First, the state-space model corresponding to the 2^{nd} -order LPF of the class-D amplifier shown in Figure C.1 can be expressed as

$$\frac{d}{dt} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} u(t), \quad (\text{C.1})$$

where $v_C(t)$ is the voltage across the capacitor C , $i_L(t)$ is the current through the inductor L , R represents the speaker resistance, and $u(t)$ is the binary-modulated signal generated by the ISMC. This control signal causes the output stage of the audio amplifier to switch between the supply voltage and ground according to the sign of the switching function (8.1):

$$u(t) = \begin{cases} V_{DD} & \text{when } s(v_e, v_i) > 0 \\ 0 & \text{when } s(v_e, v_i) < 0. \end{cases} \quad (\text{C.2})$$

The equivalent control approach [63] decomposes the discontinuous control function $u(t)$ as the sum of a high-frequency term, $u_o(t)$, and a low-frequency component,

*Reprinted with permission from “A Low-Power High-PSRR Clock-Free Current-Controlled Class-D Audio Amplifier,” by J. Torres et al., *IEEE J. Solid State Circuits*, vol. 46, issue 7, pp. 1553-1561, July 2011, © 2011 by IEEE.

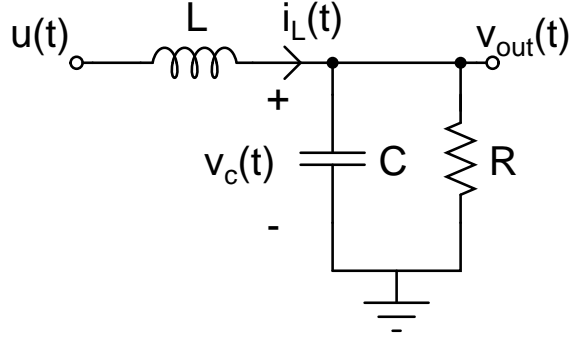


Figure C.1: Class-D amplifier output filter.

$u_{eq}(t)$, where the latter is the average value of the discontinuous function, i.e. the equivalent control input. Consequently, we have

$$u(t) = u_{eq}(t) + u_o(t). \quad (C.3)$$

Next, we calculate the input $u_{eq}(t)$ such that the states trajectories stay on the switching surface, i.e $s(v_e, v_i) = 0$. A necessary condition is that $\dot{s}(v_e, v_i) = 0$. Then, differentiating (8.1) with respect to time, using (8.4) and solving for $u(t)$ we obtain the equivalent control inputs:

$$u_{eq}(t) = \left(1 - \frac{Lk_I}{k_s R_s}\right) v_C(t) + \frac{Lk_I}{k_s R_s} v_{in}(t). \quad (C.4)$$

Substituting (C.4) into the state-space model in (C.1) we can obtain the general equivalent state-space model given by

$$\frac{d}{dt} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} = \begin{pmatrix} 0 & -\frac{k_I}{k_s R_s} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} + \begin{pmatrix} \frac{k_I}{k_s R_s} \\ 0 \end{pmatrix} v_{in}(t). \quad (C.5)$$

By definition [153], the sliding equilibrium point of the equivalent state-space model in (C.5) can be obtained if

$$\frac{d}{dt} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} = 0 \quad (\text{C.6})$$

when $s(v_e, v_i) = 0$.

Hence, the sliding equilibrium of the proposed class D audio amplifier is given by

$$v_C(t) = v_{in}(t), \quad (\text{C.7})$$

$$i_L(t) = \frac{v_{in}(t)}{R}. \quad (\text{C.8})$$

The sliding equilibrium point tracks the value of the input voltage, i.e. $v_{out}(t)$ follows $v_{in}(t)$. Similarly, the value of the output currents is defined by the ratio of the output voltage and the speaker resistance. Furthermore, the eigenvalues of the equivalent state-space model in (C.5) correspond to a stable focus since their values are complex with real negative part.

Finally, the final value theorem (FVT) [151] can calculate the steady-state response of the equivalent control state-space model to verify that a class D audio amplifier operating in sliding mode is in fact a tracking system. In general, the final value of a given system $y(t)$ can be determined as

$$\lim_{t \rightarrow \infty} y(t) = \lim_{s \rightarrow 0} sY(s). \quad (\text{C.9})$$

The transfer function of the equivalent control model, is

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{k_I/(CR_s k_s)}{s^2 + s/CR + k_I/(CR_s k_s)}, \quad (\text{C.10})$$

where k_I is defined as before and equal to $1/R_A C_A$. Applying the final value theorem to equation (C.10) with a step input of value $V_{IN}(s)$ to the system we have

$$\begin{aligned}\lim_{t \rightarrow \infty} v_{out}(t) &= \lim_{s \rightarrow 0} s V_{OUT}(s) \\ &= v_{in}(t).\end{aligned}\tag{C.11}$$

Hence, the equivalent control model tracks the input step signal $v_{in}(t)$.